Embedded Computing for
Business-Critical Continuity™

# MVME8100

## Installation and Use

P/N: 6806800P25E

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# Contact Address

Emerson Network Power - Embedded Computing

2900 South Diablo Way, Suite 190

Tempe, AZ 85282

USA

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# About this Manual

## Overview of Contents

This manual provides the information required to install and configure an MVME8100 . Additionally, this manual provides specific preparation and installation information and data applicable to the board.

The MVME8100 is a high-performance, dual core processor board featuring the Freescale QorIQ P5020 processor.

This manual is divided into the following chapters and appendices:

Chapter 1, *Introduction*, lists the features of the MVME8100 baseboard, standard compliances, and model numbers for boards and accessories.

Chapter 2, *Hardware Preparation and Installation*, includes a description of the MVME8100, unpacking instructions, environmental, thermal, and power requirements, and how to prepare and install the baseboard, transition module, and PMC module.

Chapter 3, *Controls, LEDs, and Connectors*, provides an illustration of the board components and front panel details. This chapter also gives descriptions for the onboard and front panel LEDs and connectors.

Chapter 4, *Functional Description*, describes the major features of the MVME8100 baseboard. These descriptions include both programming and hardware characteristics of major components.

Chapter 5, *Boot System, on page 89*, describes the boot load software.

Appendix A, *Battery Exchange*, describes the procedure for replacing a battery.

Appendix B, *Related Documentation*, provides listings for publications, manufacturer's documents and related industry specification for this product.

*Safety Notes*, contains the cautions and warnings applicable to the use of this product.

*Sicherheitshinweise*, is a German translation of the Safety Notes chapter.

# Abbreviations

This document uses the following abbreviations:

| TERM | MEANING |
|---|---|
| A | Amps |
| AC | Alternating Current |
| ANSI | American National Standard Institute |
| BGA | Ball Grid Array |
| BLT | Block Transfer |
| CCB | Core Complex Bus |
| CE | Chip Enable |
| CFM | Cubic Feet per Minute |
| CMC | Common Mezzanine Card |
| COM | Communications |
| COP | Common On-chip Processor |
| CPLD | Complex Programmable Logic Device |
| CPU | Central Processing Unit |
| CRC | Cyclic Redundancy Check |
| DC | Direct Current |
| DDR | Double Data Rate |
| °C | Degrees Celsius |
| DIMM | Dual In-line Memory Module |
| DMA | Direct Memory Access |
| DRAM | Dynamic Random Access Memory |
| ECC | Error Correction Code |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| eMMC | Enhanced Module Management Controller |
| FCC | Federal Communications Commission |
| FIFO | First In First Out |

| TERM | MEANING |
|---|---|
| fpBGA | Flip chip Plastic Ball Grid Array |
| GB | Gigabytes |
| Gbit | Gigabit |
| Gbps | Gigabits Per Second |
| GMII | Gigabit Media Independent Interface |
| ID | Identification |
| I/O | Input/Output |
| IEEE | Institute of Electrical and Electronics Engineers |
| I2C | Inter IC |
| IWD | Initial Hardware Watchdog |
| JTAG | Joint Test Access Group |
| KB | Kilobytes |
| KBAUD | Kilo Baud |
| LBC | Local Bus Controller |
| LCD | Liquid Crystal Display |
| LED | Light Emitting Diode |
| MB | Megabytes |
| Mbit | Megabit |
| Mbps | Megabits Per Second |
| MHz | Megahertz |
| MII | Media Independent Interface |
| MRAM | Magnetoresistive random-access memory |
| NAND | (Not and) Flash that is used for storage |
| OS | Operating System |
| OSWD | OS Watchdog |
| PBGA | Plastic Ball Grid Array |
| PCI | Peripheral Component Interconnect |
| PCI-X | Peripheral Component Interconnect -X |

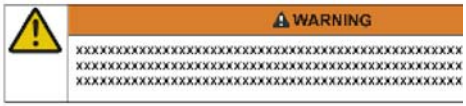
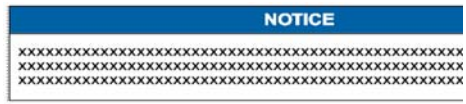
| TERM | MEANING |
|---|---|
| PIC | Programmable Interrupt Controller |
| PIM | PCI Mezzanine Card Input/Output Module |
| PMC | PCI Mezzanine Card (IEEE P1386.1) |
| PLD | Programmable Logic Device |
| PLL | Phase-Locked Loop |
| POR | Power-On Reset |
| PrPMC | Processor PCI Mezzanine Card |
| QUART | Quad Universal Asynchronous Receiver/Transmitter |
| RAM | Random Access Memory |
| RGMII | Reduced Gigabit Media Independent Interface |
| ROM | Read-Only Memory |
| RTC | Real-Time Clock |
| RTM | Rear Transition Module |
| sATA | Serial AT Attachment |
| SBC | Single Board Computer |
| SDRAM | Synchronous Dynamic Random Access Memory |
| SMT | Surface Mount Technology |
| SODIMM | Small-Outline Dual In-line Memory Module |
| SPD | Serial Presence Detect |
| SRAM | Static Random Access Memory |
| TSEC | Three-Speed Ethernet Controller |
| 2eSST | Two edge Source Synchronous Transfer |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |
| V | Volts |

| TERM | MEANING |
|---|---|
| VITA | VMEbus International Trade Association |
| VME | VMEbus (Versa Module Eurocard) |
| VPD | Vital Product Data |
| W | Watts |

# Conventions

The following table describes the conventions used throughout this manual.

| Notation | Description |
|---|---|
| 0x00000000 | Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets |
| 0b0000 | Same for binary numbers (digits are 0 and 1) |
| bold | Used to emphasize a word |
| `Screen` | Used for on-screen output and code related elements or commands in body text |
| **`Courier + Bold`** | Used to characterize user input and to separate it from system output |
| *Reference* | Used for references and for table and figure descriptions |
| File > Exit | Notation for selecting a submenu |
| <text> | Notation for variables and keys |
| [text] | Notation for software buttons to click on the screen and parameter description |
| ... | Repeated item for example node 1, node 2, ..., node 12 |
| .<br>.<br>. | Omission of information from example/command that is not necessary at the time being |
| .. | Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers) |

| Notation | Description |
|---|---|
| \| | Logical OR |
|  | Indicates a hazardous situation which, if not avoided, could result in death or serious injury |
| | Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury |
|  | Indicates a property damage message |
| | No danger encountered. Pay attention to important information |

# Summary of Changes

This is the first edition of the MVME8100 Single Board Computer Installation and Use.

| Part Number | Publication Date | Description |
|---|---|---|
| 6806800P25A | May 2012 | First edition |
| 6806800P25B | November 2012 | GA release |
| 6806800P25C | December 2012 | Updated *Standard Compliances* on page 22 |
| 6806800P25D | September 2013 | Updated Table 1-2, Table 1-3, Table 2-2, Table 2-4, *PMC/XMC Installation* on page 38, Table 3-3 on page 50, and Table 3-6 on page 53.<br>Added Figure 2-2 on page 32, *SATA Installation* on page 41, Figure 2-4 on page 43, Figure 3-2 on page 48, *Interrupt Controller Assignments* on page 86 and *GPIO Electrical Characteristics* on page 87. |
| 6806800P25E | December 2013 | Added Chapter 5, *Boot System, on page 89*. |

## 1.1 Features

The MVME8100 Single Board Computer is a VMEbus board based on the Freescale QorIQ P5020 processor. It is a high performance 6U VME/VXS board targeted towards high-end military and industrial automation applications using VMEbus. The MVME8100 is compliant with the VITA standards VMEbus, 2eSST, and PCI-X.

*Table 1-1 Features List*

| Function | Features |
|---|---|
| Processor<br>(Subset of P5020 features used on MVME8100) | • Freescale QorIQ P5020<br>• Two e5500 Power Architecture cores<br>• Five Gigabit Ethernet controllers (SGMII and RGMII interfaces)<br>• Two 64-bit DDR3/3L SDRAM memory controllers with ECC<br>• Multicore Programmable Interrupt Controller (PIC)<br>• Four I2C controllers<br>• Two 4-pin UARTs<br>• Two 4-channel DMA engines<br>• Enhanced local bus controller (eLBC)<br>• Two PCI Express controller/ports<br>• One Serial Rapid IO controller/ports (SRIO port) v1.3-compliant with features of v2.1<br>• Enhanced secure digital host controller (SD/MMC)<br>• Enhance Serial Peripheral Interfaces (eSPI)<br>• Two high-speed USB 2.0 controllers with integrated PHYs |
| System Memory | • Two banks of DDR3 SDRAM with ECC<br>• Total 4 GB (2GB per Bank)<br>• 1333 MHz DDR3 data rate |
| SM Bus | • One 512 Kbit user configuration serial EEPROM<br>• 256B SPD EEPROMs<br>• One 64 Kbit VPD EEPROM<br>• RTC with battery backup<br>• Temperature Sensors<br>• RTM and XMC VPD EERPOMs |

*Table 1-1 Features List (continued)*

| Function | Features |
|---|---|
| FLASH | • Two soldered SPI FLASH, 8MB each, switchable for uboot primary/backup support<br>• Hardware switch or Software bit write protection for entire logical bank<br>• Eight GB eMMC Flash |
| NVRAM | 512 KB MRAM |
| PCI Express | • Two 4X Ports to VXS backplane P0 (muxed with SRIO ports)<br>• One 8X Port to PMC/XMC Site 1<br>• One 4X Port to PMC/XMC Site 2 |
| SRIO | Two 4X Ports to VXS backplane P0 (muxed with PCIe ports) |
| USB | • One USB 2.0 for front panel I/O<br>• Two USBs 2.0 for backplane RTM I/O |
| Ethernet | • One 10/100/1000BASE-T Ethernet port to front panel (only in air cooled variant)<br>• Two 10/100/1000BASE-T Ethernet channels to P2 / RTM<br>• Two 1000BASE-BX Ethernet SERDES channels to P0 backplane / RTM |
| Serial Ports | • One RS232/422/485 console port to front panel or P2 / RTM<br>• Up to 4 RS232/422/485 COM ports to P2/ RTM |
| VME Bus | VME64x and 2eSST |
| Timers | • Eight 32-bit timers in CPU<br>• Watchdog timer in CPU |
| PMC/XMC | Two PMC/XMC sites with 64-bit PMCIO on Site 1 |
| SATA SSD | Option for one 2.5 inch SATA drive (PMC/XMC Site 2) |
| GPIO Interface | Four GPIOs to RTM |
| VXS Interface | • VXS (VITA 41) Specification compliant<br>• Support backplane P0 connector |
| Form Factor | • Standard 6U, one slot<br>• Support 0.8, and 0.85 inch slot chassis<br>• Support heat frame on both sides for Conduction cooled board |

*Table 1-1 Features List (continued)*

| Function | Features |
|---|---|
| Miscellaneous | • One front panel RESET Switch<br>• LED front panel status indicators: four user/fail/ready LEDs<br>• Planar status indicators<br>• Boundary scan support |
| Software Support | • VxWorks OS support<br>• Linux OS support |
| RTM | Compatible with RTM (assembly # 0106852M***) |
| I/O | • One micro DB9 connector for console port on front panel<br>• One USB2.0 type A connector on front panel<br>• One front panel RJ45 connector with integrated LEDs for 10/100/1000 Ethernet channel<br>• PMC/XMC site 1 front I/O and rear PMC I/O<br>• PMC/XMC site two front I/O<br>• Four Serial ports to P2/RTM, two with micro DB9 connectors on RTM panel and two on planar headers<br>• Two 10/100/1000BASE-T Ethernet channels to RJ45 connectors on RTM panel<br>• Two 1000 BASE-BX Ethernet SERDES channels to backplane<br>• Two USB2.0 ports to RTM with USB type A connectors on RTM panel<br>• One SATA port to RTM with eSATA connector on RTM<br>• Four GPIOs to planar headers on RTM<br>Note: The front panel I/O connectors are available only in ENP1 (air cooled variants). I/O signals in ENP4 (conduction cooled) variant are accessed through P2 only. |

## 1.2 Standard Compliances

The MVME8100 is designed to be CE compliant and to meet the following standard requirements.

*Table 1-2 Board Standard Compliances*

| Standard | Description |
|---|---|
| UL 60950-1<br>EN 60950-1<br>IEC 60950-1<br>CAN/CSA C22.2 No 60950-1 | Safety Requirements (legal) |
| CISPR 22<br>EN 55022<br>EN 55024<br>FCC Class A<br>VCCI Japan<br>AS/NZS CISPR 22 | EMC requirements (legal) on system level (predefined Emerson system) |
| ETSI EN 300 019 series | Environmental Requirements |
| Directive 2002/95/EC | Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS).<br>The ENP1 version complies with RoHs 6 of 6. The ENP4 version complies with RoHS 5 of 6 due to lead solder used in the ENP4 heat frame. |

For Declaration of Conformity, refer MVME8100 DOC.

## 1.3 Mechanical Data

The MVME8100 is a full 6U board with added mounting holes to support an ENP4 board variant. The MVME8100 will occupy a single VME card slot.

Table 1-3 provides details on the board's mechanical data.

*Table 1-3 Mechanical Data*

| Characteristic | Value |
|---|---|
| Height | 233.44 mm (9.2inches) |
| Depth | 160.0 mm (6.3 inches) |
| Front Panel Height | 261.8 mm (10.3 inches) |
| Width | 19.8 mm (0.8 inches) |
| Maximum Component Height | 14.8 mm (0.58 inches) |
| Weight (estimated) | 0.58 Kg (ENP1)<br>0.90 Kg (ENP4) |

## 1.4 Ordering Information

When ordering board variants or board accessories, use the order numbers given in the following tables.

### 1.4.1 Supported Board Models

*Table 1-4 Board Variants*

| Marketing # | Processor |
|---|---|
| MVME8100-202200401E | P5020 2.0GHz 28W, 4GB DDR3, VXS, 2 PMC/XMC, IEEE, ENP1 |
| MVME8100-202200401S | P5020 2.0GHz 28W, 4GB DDR3, VXS, 2 PMC/XMC, SCANBE, ENP1 |
| MVME8100-202200404 | P5020 1.8GHz 27W, 4GB DDR3, VXS, 2 PMC/XMC, ENP4 |

## 1.4.2 Board Accessories

This table lists the available expansion and transition modules for the MVME8100.

| Model Number | Description |
|---|---|
| VXS1-RTM1 | RTM for MVME8100 (supports ENP1 specifications only) |
| MVME8100-HDMNTKIT4 | SSD Mounting kit (HDD not included) |

.

# Hardware Preparation and Installation

## 2.1 Overview

This chapter provides startup and safety instructions related to this product, hardware preparation instruction that includes default switch settings. System considerations and installation instructions for the baseboard, PMC, XMC, and Rear Transition Module (RTM) are also described in this chapter.

A fully implemented MVME8100 consists of the baseboard plus:

- Two single-wide or one double-wide PCI Mezzanine Card (PMC) slot for added versatility.
- One rear transition module for support of the mapped I/O from the MVME8100 baseboard to the P2 connector.
- Up to two optional XMC cards (in place of PMC modules).

The following table lists the things you need to do before using this board and explains where you can find the information for performing each step. Be sure to read this entire chapter, including all Caution and Warning notes, before you begin.

*Table 2-1 Startup Overview*

| Task | Page |
|---|---|
| Unpack the hardware. | *Unpacking and Inspecting the Board* on page 26 |
| Configure the hardware by setting jumpers on the board and RTM. | *Configuring the Board* on page 30 |
| Install the RTM (VXS1-RTM1) of MVME8100 in the chassis. | *Rear Transition Module* on page 37 |
| Install PMC module (if required). | *Installing Accessories* on page 37 |
| Install XMC module (if required). | *Installing Accessories* on page 37 |
| Install the MVME8100 in the chassis. | *Installing and Removing the Board* on page 44 |
| Attach cabling and apply power. | *Completing the Installation* on page 46 |
| Install PIM on transition module (if required). | Refer *VXS1-RTM1 Installation and Use* manual. |
| Examine and/or change environmental parameters. | *MVME8100 Single Board Computer Programmer's Reference* |
| Program the board as needed for your applications. | *MVME8100 Single Board Computer Programmer's Reference* |

## 2.2 Unpacking and Inspecting the Board

Read all notices and cautions prior to unpacking the product.

**NOTICE**

Damage of Circuits
Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.
Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

### Shipment Inspection

To inspect the shipment, perform the following steps:

1. Verify that you have received all items of your shipment.
2. Check for damage and report any damage or differences to customer service.
3. Remove the desiccant bag shipped together with the board and dispose of it according to your country's legislation.

The product is thoroughly inspected before shipment. If any damage occurred during transportation or any items are missing, contact customer service immediately.

## 2.3 Requirements

Make sure that the board, when operated in your particular system configuration, meets the requirements specified in the next sections.

### 2.3.1 Environmental Requirements

The following table lists the currently available specifications for the environmental characteristics of the MVME8100. A complete functional description of the MVME8100 baseboard appears in Chapter 4, *Functional Description*.

The MVME8100 has ENP1 and ENP4 variants which comply with the following environmental and regulatory specifications.

For ENP1 boards, the operating temperatures refer to the temperature of the air circulating around the board and not to the component temperature.

For ENP4 board, the operating temperature refers to the temperature at the card edge frame.

*Table 2-2 MVME8100 Specifications*

| Characteristics | ENP1 | ENP4 |
|---|---|---|
| Cooling Method | Forced Air | Conduction |
| Operating temperature | 0°C to +55°C | –40°C to +85° C |
| Storage Temperature | -40°C to +85°C | -55°C to +105°C<br>Note: The MVME8100 ENP 4 version includes NAND Flash memory in the form of the eMMC. The specified storage limits for the MVME8100 ENP 4 version are -55°C to +105°C. However, it should be noted that the industry standard (for Flash) as well as the specific vendor of this component only warrants performance (without data degradation) from -40°C to +85°C. Storage of the MVME8100 outside this range (while supported by other components on the board) may result in an unspecified reduction in the data retention capabilities of the eMMC. |
| Relative humidity | To 95% RH | To 100% RH |
| Vibration Sine (10min/axis) | 2G, 5 to 500Hz | 10G, 15 to 2000Hz |
| Vibration Random (1hr/axis) | .002g/Hz, 15 to 2000Hz(2G RMS) | 0.1g/Hz, 15 to 2000Hz (12GRMS) |

*Table 2-2 MVME8100 Specifications (continued)*

| Characteristics | ENP1 | ENP4 |
|---|---|---|
| Shock | 20g/11mS | 40g/11mS |
| Conformal Coating | No | Option (Acrylic) |

**NOTICE**

Product Damage
High humidity and condensation on the board surface causes short circuits.
Do not operate the board outside the specified environmental limits.
Make sure the board is completely dry and there is no moisture on any surface before applying power.

## 2.3.2 Power Requirements

The MVME8100 uses the backplane +5V source to power each on board power supply. The +3.3V backplane supply is not utilized in order to have backward compatibility with old 3-row chassis. The -12V and +12V is routed through to the XMC and PMC connectors. The power estimates provided in the following table is the total board consumption from +5V, excluding the PMC/XMC, SATA HDD/SSD and USB devices.

*Table 2-3 Operating Voltages*

| Voltages | Minimum | Normal | Maximum |
|---|---|---|---|
| +5.0V | 4.875V (-2.5%) | 5.0V | 5.25V (+5%) |

*Table 2-4 Power Requirements*

| Board Variant | Power |
|---|---|
| MVME8100-202200401S/E<br>(ENP1) | Board idle at OS prompt: 38 Watts, typical<br>Operating load*: 42 Watts, typical<br>54 Watts, Max(@55°C)<br>* Operating conditions: No RTM, PMC/XMC or peripherals. |

*Table 2-4 Power Requirements*

| Board Variant | Power |
|---|---|
| MVME8100-202180404<br>(ENP4) | Operating load*: 65 Watts, max (@85°C card edge temperature) |

The following table shows the power limits due to the available 5 volts pins, when the MVME8100 is installed in either a 3-row or 5-row chassis and when PMCs/XMCs are present.

| Chassis Type | Power Limit | Power limits PMCs or XMCs |
|---|---|---|
| 3-Row | 70 W maximum | Below 70 W[1] |
| 5-Row | 90 W maximum | Below 90 W[1] |

1. Keep below power limit. Cooling limitations must be considered.

## 2.3.3 Thermal Requirements

The MVME8100 module requires a minimum air flow of 10 CFM uniformly distributed across the board, with the airflow traveling in the direction from PMC/XMC 1 to PMC/XMC 2, when operating at a 55°C (131°F) ambient temperature.

## 2.3.4 Thermally Significant Components

The chassis into which the MVME8100 is installed must provide sufficient airflow to maintain proper board operating temperature. The P5020 processor temperature should be monitored while the board is operational to ensure that the processor core temperature does not exceed 100°C. The processor core temperature can be read using the I2C sensor at address 0x4C on the processor I2C bus #1. For more information, refer *MVME8100 Single Board Computer Programmer's Reference*.

### 2.3.5 Equipment Requirements

The following equipment is recommended to complete an MVME8100 system:

- VMEbus system enclosure
- System console terminal
- Operating system (and/or application software)

## 2.4 Configuring the Board

To produce the desired configuration and ensure proper operation of the MVME8100, you may need to carry out certain hardware modifications before installing the module.

The MVME8100 provides software control over most options: by setting bits in control registers after installing the module in a system, you can modify its configuration.

Prior to installing PMC modules on the MVME8100 baseboard, ensure that all switches that are user configurable are set properly. To do this, refer to Figure 2-1 or the board itself, for the location of specific switches and set the switches according to the following descriptions.

*Figure 2-1 Switch Locations (ENP1 board)*

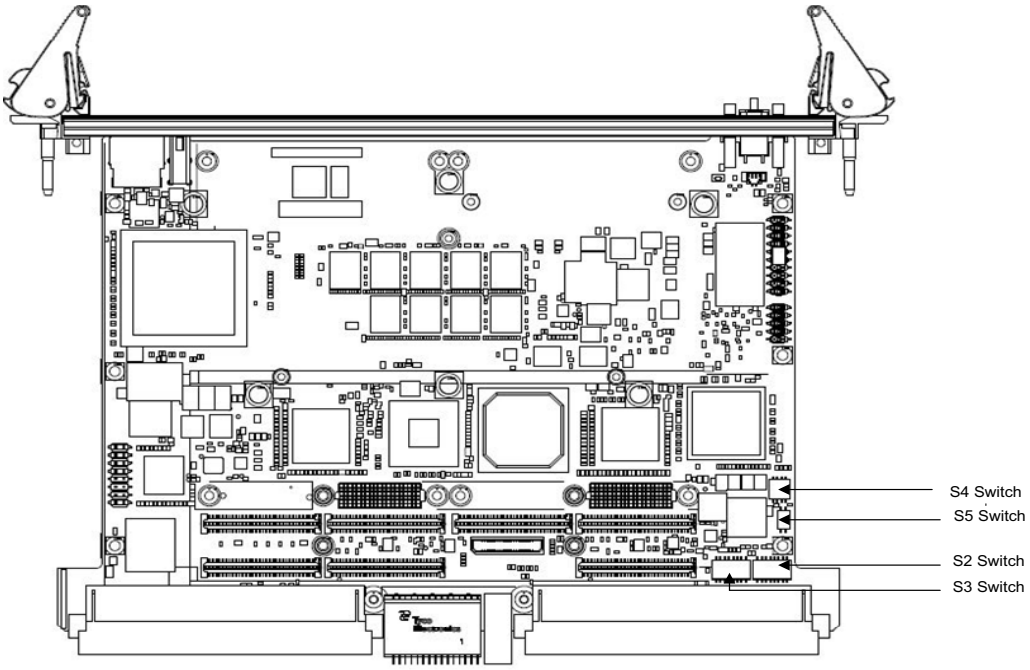
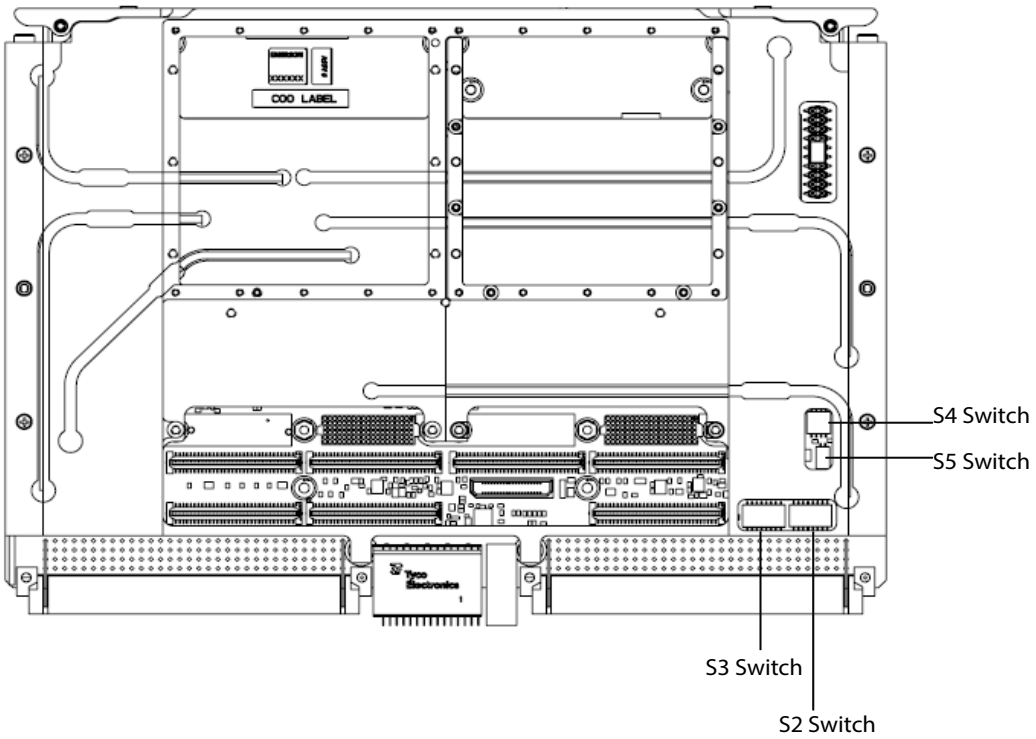


*Figure 2-2 Switch Locations (ENP4 Board)*




The following sections describe the on-board switches and their configurations for the MVME8100.

**NOTICE**

Board Malfunction
Switches marked as “reserved” might carry production-related functions and can cause the board to malfunction if their setting is changed.
Do not change settings of switches marked as “reserved”. The setting of switches which are not marked as “reserved” has to be checked and changed before board installation.

## 2.4.1 Configuration Switches

The board provides the following configuration switches:

- S2 Switch
- S3 Switch
- S4 Switch
- S5 Switch
- Reset/Abort Switch

### 2.4.1.1 S2 Switch

The Switch Bank S2 provides watchdog control, serial port configuration and P0 fabric selection.

*Table 2-5 S2 Switch Settings*

| Position | Default | Description |
|---|---|---|
| 1 | OFF | OFF - Watchdog Disabled<br>ON - Watchdog Enabled |
| 2 | OFF | OFF - Serial Console Port to Front Panel<br>ON - Serial Console Port to P2/RTM panel |
| 3 | OFF | OFF - P2 Serial Port 0 is RS232<br>ON - P2 Serial Port 0 is RS422/485 |
| 4 | OFF | OFF - P2 Serial Port 1 is RS232<br>ON - P2 Serial Port 1 is RS422/485 |
| 5 | OFF | OFF - P2 Serial Port 2 is RS232<br>ON - P2 Serial Port 2 is RS422/485 |
| 6 | OFF | OFF - P2 Serial Port 3 is RS232<br>ON - P2 Serial Port 3 is RS422/485 |
| 7 | OFF | OFF - Front Panel console Port is RS232<br>ON - Front Panel console Port is RS422/485 |
| 8 | OFF | OFF - Select SRIO for P0 Backplane Fabric<br>ON - Select PCIe for P0 Backplane Fabric |

### 2.4.1.2 S3 Switch

The TSI148 VMEbus Status Register provides the VMEbus geographical address of the MVME8100. Applications not using a 5-row backplane can use these switches to manually assign board's VMEbus geographical address. Note that this switch is wired parallel with geographical address pins on the 5-row connector to these switches must be in the off position when installed in a 5-row chassis in order to get the correct address from P1 connector. This switch reflects the inverted states on the geographical address signals.

*Table 2-6 S3 Switch Settings*

| Position | Default | Description |
|---|---|---|
| 1 | OFF | OFF - SPI FLASH Write Protect is Disabled<br>ON - SPI FLASH Write Protect is Enabled |
| 2 | OFF | P0 Connector Port B PCIE/SRIO Fabric Selection<br>OFF- Port B same as Port A selection and is controlled by SW2-8<br>ON - Port B selection is opposite of SW2-8 selection |
| 3 | OFF (1) | GAP# |
| 4 | OFF (1) | GA4# |
| 5 | OFF (1) | GA3# |
| 6 | OFF (1) | GA2# |
| 7 | OFF (1) | GA1# |
| 8 | OFF (1) | GA0# |

Below is the switch configuration for corresponding slot address in a 21 slot chassis 3-row backplane.

*Table 2-7 Three Row Backplane Manual Slot Addressing*

| S1-3 | S1-4 | S1-5 | S1-6 | S1-7 | S1-8 | GAP# GA(4:0)# | Slot Address |
|---|---|---|---|---|---|---|---|
| OFF | OFF | OFF | OFF | OFF | ON | 1 11110 | 1 |
| OFF | OFF | OFF | OFF | ON | OFF | 1 11101 | 2 |
| ON | OFF | OFF | OFF | ON | ON | 0 11100 | 3 |
| OFF | OFF | OFF | ON | OFF | OFF | 1 11011 | 4 |

*Table 2-7 Three Row Backplane Manual Slot Addressing*

| S1-3 | S1-4 | S1-5 | S1-6 | S1-7 | S1-8 | GAP# GA(4:0)# | Slot Address |
|---|---|---|---|---|---|---|---|
| ON | OFF | OFF | ON | OFF | ON | 0 11010 | 5 |
| ON | OFF | OFF | ON | ON | OFF | 0 11001 | 6 |
| OFF | OFF | OFF | ON | ON | ON | 1 11000 | 7 |
| OFF | OFF | ON | OFF | OFF | OFF | 1 10111 | 8 |
| ON | OFF | ON | OFF | OFF | ON | 0 10110 | 9 |
| ON | OFF | ON | OFF | ON | OFF | 0 10101 | 10 |
| OFF | OFF | ON | OFF | ON | ON | 1 10100 | 11 |
| ON | OFF | ON | ON | OFF | OFF | 0 10011 | 12 |
| OFF | OFF | ON | ON | OFF | ON | 1 10010 | 13 |
| OFF | OFF | ON | ON | ON | OFF | 1 10001 | 14 |
| ON | OFF | ON | ON | ON | ON | 0 10000 | 15 |
| OFF | ON | OFF | OFF | OFF | OFF | 1 01111 | 16 |
| ON | ON | OFF | OFF | OFF | ON | 0 01110 | 17 |
| ON | ON | OFF | OFF | ON | OFF | 0 01100 | 18 |
| OFF | ON | OFF | OFF | ON | ON | 1 01100 | 19 |
| ON | ON | OFF | ON | OFF | OFF | 0 01011 | 20 |
| OFF | ON | OFF | ON | OFF | ON | 1 01010 | 21 |

### 2.4.1.3 S4 Switch

The S4 switch includes the SCON control and PCIE/SRIO P0 root complex/endpoint configuration switches. The VME SCON AUTO switch is OFF to select Auto-SCON mode. The switch is ON to select manual SCON mode which works in conjunction with the VME SCON SEL switch. The VME_SCON_SEL switch is OFF to manually select SCON mode. This switch is ON to manually select non-SYSCON mode. This switch is only effective when the VME SCON AUTO switch is ON.

*Table 2-8 S4 Switch Settings*

| Position | Default | Description |
|---|---|---|
| 1 | OFF | Clear Environment Variables<br>OFF - Disable Clear Environment Variables<br>ON - Enable Clear Environment Variables. At reset, uboot ENV variables are set to default values. |
| 2 | OFF | OFF - Configure PCIe/SRIo Switches as P0 Root Complex<br>ON - Configure PCIe/SRIO Switches as P0 Endpoint |
| 3 | OFF | OFF - Auto VME System Controller<br>ON - Manual VME System Controller |
| 4 | OFF | OFF - VME System Controller<br>ON - VME Non-System Controller |

### 2.4.1.4 S5 Switch

The switch Bank S5 provides the boot SPI FLASH selection.

*Table 2-9 S5 Switch Settings*

| Position | Default | Description |
|---|---|---|
| 1 | OFF | OFF - Boot from SPI FLASH 0<br>ON - Boot from SPI FLASH 1 |
| 2 | OFF | Reserved |

#### 2.4.1.5 Reset /Abort Switch

A dual function switch can be found in the front panel. This switch can function either as a Reset or Abort button. If the button is pressed for less than 3 seconds, the CPLD will generate an abort interrupt to the P5020 processor. If the button is pressed for more than 3 seconds, the CPLD will generate a board hard reset. If the board is configured as System Controller, the backplane VME SYSRESET signal is also asserted during a board hard reset.

## 2.5 Installing Accessories

This section describes the procedures for installing the RTM of MVME8100, PMCs, and the XMCspan on the baseboard.

### 2.5.1 Rear Transition Module

The RTM of MVME8100 does not support hot swap, You must remove power to the system before installing the module. Before installing the transition module, you may need to manually configure the RTM switches and install a PMC I/O Module (PIM).

**NOTICE**

Damage of Circuits
Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.
Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

Product Damage
Only use injector handles for board insertion to avoid damage to the front panel and/or PCB. Deformation of the front panel can cause an electrical short or other board malfunction.

Board Malfunction
Switches marked as “reserved” might carry production-related functions and can cause the board to malfunction if their setting is changed.
Do not change settings of switches marked as “reserved”. The setting of switches which are not marked as “reserved” has to be checked and changed before board installation.

### Installation and Removal Procedure

To begin the installation of the RTM in a chassis, proceed as follows:

1. Turn all equipment power OFF and disconnect the power cable from the AC power source.
2. Remove the chassis cover as instructed in the equipment user's manual.
3. Remove the filler panel(s) from the appropriate card slot(s) at the rear of the chassis (if the chassis has a rear card cage).
4. Install the top and bottom edge of the RTM into the rear guides of the chassis.
5. Ensure that the levers of the two injector/ejectors are in the outward position.
6. Slide the RTM into the chassis until resistance is felt.
7. Simultaneously move the injector/ejector levers in an inward direction.
8. Verify that the RTM is properly seated and secure it to the chassis using the two screws located adjacent to the injector/ejector levers.
9. Connect the appropriate cables to the RTM.

To remove the RTM from the chassis, reverse the procedure and press the red locking tabs (IEEE handles only) to extract the board.

## 2.5.2 PMC/XMC Installation

The PMC connectors are placed to support two single-width PMCs or one double-width PMC. PMC site 1 supports front PMC I/O and rear PMC I/O via the Jn4 connector. PMC 1 I/O is routed to the VME P2 connector. PMC site 2 only supports front PMC I/O and does not have a Jn4 connector. The PMC 1 Jn4 user I/O signals only support low-current high-speed signals and thus do not support current-bearing power supply usage.

The user-configured switches are accessible with the PMC/XMCs installed. The onboard PMC sites are configured to support +3.3 V I/O PMC modules. The onboard PMC sites do not support +5.0 V I/O PMC modules.

The ENP4 version only supports rugged conduction cooled PMC/XMC modules (see VITA 20-2001 for conduction cooled PMC for mechanical definition.

Follow these steps to install a PMC/XMC module onto the MVME8100 board.

### Installation Procedure

Read all notices and follow these steps to install a PMC/XMC on the baseboard.

**NOTICE**

Logic Ground to Chassis Ground Isolation
The MVME8100 ENP1 and ENP4 heat frames are isolated from the board logic ground. Installing a PMC or XMC module which has mounting locations connected to the module logic ground will result in a short between chassis ground and the MVME8100 logic ground.

Damage of Circuits
Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.
Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

Product Damage
Inserting or removing modules with power applied may result in damage to module components.
Before installing or removing additional devices or modules, read the documentation that came with the product.

1. Attach an ESD strap to your wrist. Attach the other end of the strap to the chassis as a ground. Make sure that it is securely fastened throughout the procedure.
2. If the PMC/XMC has a front filler panel, remove the PMC/XMC filler plate from the front panel cut-out.
3. Remove the two rear stand-offs from the PMC/XMC. The MVME8100 heat frame has built-in rear stand-offs.

4. Slide the front bezel of the PMC/XMC into the cut-out from behind. The front bezel of the PMC/XMC module will be flushed with the board when the connectors on the module align with the mating connectors on the board.
   Note: ENP4 PMC/XMC modules do not have front bezels.

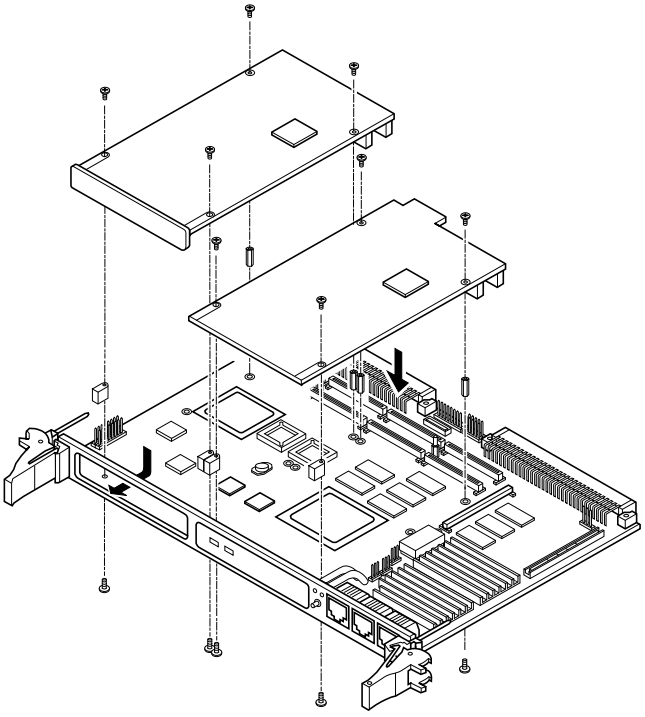
5. Align the mating connectors properly and apply minimal pressure to the PMC/XMC until it is seated to the board.

6. Insert the two front PMC/XMC mounting screws through the mounting holes on the bottom side of the board, and then install the top side screws. Tighten the screws.
   Note: Rugged PMC/XMC modules installed on an ENP4 MVME8100 have more than four mounting screws.

7. Install the board into the appropriate card slot. Make sure that the board is well seated into the backplane connectors. Do not damage or bend connector pins.

8. Replace the chassis or system cover.
9. Reconnect the system to the power source and then turn on the system.

*Figure 2-3 Typical Placement of a PMC/XMC Module on a VME Module*



## 2.5.3 SATA Installation

A 2.5" SATA drive can be installed in PMC/XMC site 2. The MVME8100-HDMTKIT4 SATA mounting kit (6706881A01x) provides the mounting hardware. A SATA drive which meets the intended board operating environment for temperature and vibration must be used.

Read all notices and follow these steps to install a SATA drive on the baseboard.

**NOTICE**

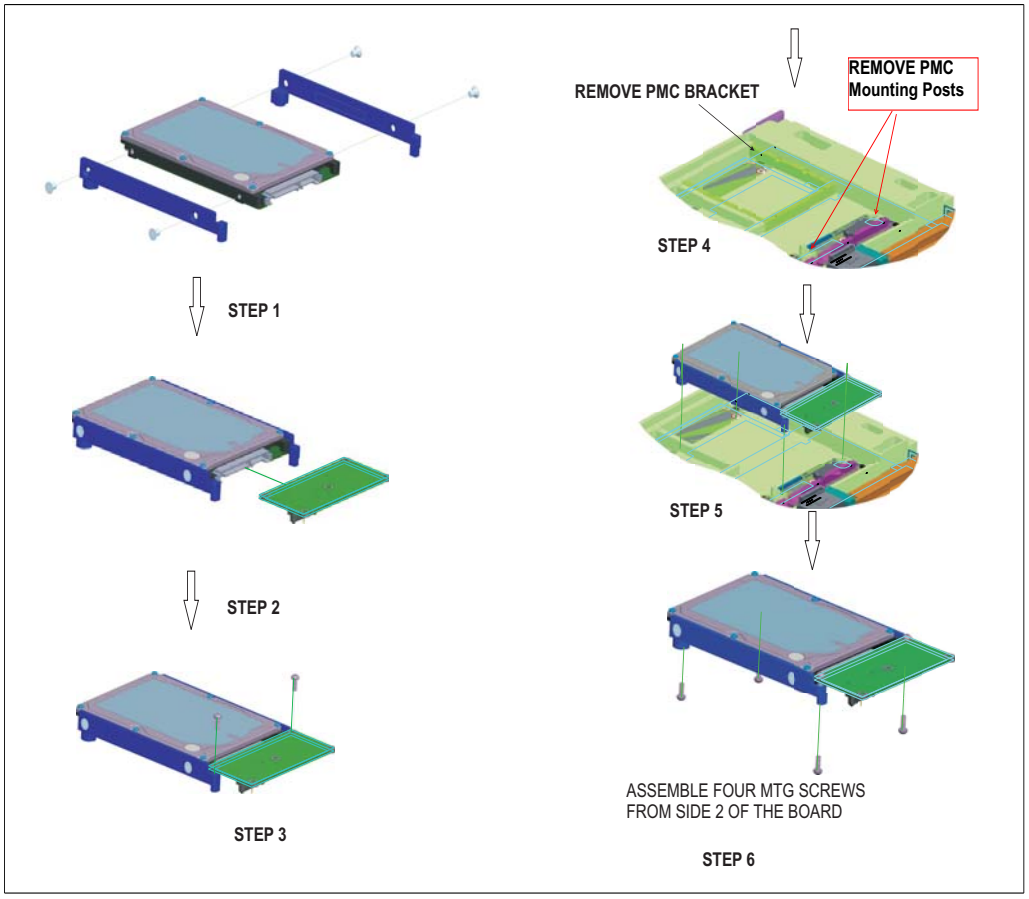
Logic Ground to Chassis Ground Isolation

The MVME8100 ENP1 and ENP4 heat frames are isolated from the board logic ground. Installing a SATA drive which has a metallic case connected to the drive logic ground will result in a short between chassis ground and the MVME8100 logic ground.

Damage of Circuits
Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.
Before touching the board or electronic components, make sure that you are working in an ESD- safe environment.

Product Damage
Inserting or removing modules with power applied may result in damage to module components.
Before installing or removing additional devices or modules, read the documentation that came with the product.

*Figure 2-4 SATA drive Installation*




Use the following steps to install a SATA drive:

1. Wear an ESD strap to your wrist and fix the other end of the ESD strap to an electrical ground.
2. Secure mounting brackets to each side of SATA drive as shown in step 1 of Figure 2-4.
3. Attach SATA adapter board to SATA drive as shown in step 2 of Figure 2-4.
4. Use two screws to secure adapter to mounting brackets as shown in step 3 of Figure 2-4.

5. Remove PMC/XMC bracket and mounting posts from site 2 as shown in step 4 of Figure 2-4.
6. Attach SATA drive assembly with adapter board and mounting brackets to MVME8100 board at PMC/XMC site 2 as shown in step 5 of Figure 2-4. Make sure that the SATA adapter connector is fully mated with the board SATA connector.
7. Secure SATA drive assembly to board using four screws inserted from the bottom side of the board as shown in step 5 of Figure 2-4.

## 2.6 Installing and Removing the Board

This section describes the recommended procedure for installing the MVM8100 board in a chassis. The MVME8100 does not support hot swap, you must remove power to the slot or system before installing the module. Before installing the MVME8100, ensure that the serial ports and switches are properly configured.

### Installation and Removal Procedure

Before you install your module, please read all cautions, warnings and instructions presented in this section.

**NOTICE**

Damage of Circuits
Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.
Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

Product Damage
Only use injector handles for board insertion to avoid damage to the front panel and/or PCB. Deformation of the front panel can cause an electrical short or other board malfunction.

Use the following steps to install the MVME8100 into your computer chassis.

1. Wear an ESD strap to your wrist.
2. Attach the other end of the ESD strap to an electrical ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
3. Remove any filler panel that might fill the slot.
4. Install the top and bottom edge of the MVME8100 into the guides of the chassis.
5. Ensure that the levers of the two IEEE locking injector/ejectors (if equipped) are in the unlocked outward position.
6. Slide the MVME8100 into the chassis until you feel resistance.
7. Simultaneously move the injector/ ejector levers (if equipped) in an inward direction until locked. If fitted with SCANBE ejectors, adjust them inward and apply pressure to them to seat the board.
8. Verify that the MVME8100 is properly installed and secure it to the chassis using the two screws located adjacent to the injector/ejector levers.
9. When installing an ENP4 version board, the maximum torque that should be used on the wedge lock screws is 6 in-lbs.
10. Connect the appropriate cables to the MVME8100.

When the MVME8100 (and optionally, an RTM) is installed in a chassis, you are ready to connect peripherals and apply power to the slot or system.

The front-panel Micro-DB9 connector provides a console interface to U-boot. It presents an RS-232 DTE interface (TX/RX/ CTS/RTS). The default serial configuration is 9600/8/N/1. This mates with an ITT MDSM-9SC-Z11 (or equivalent). The Emerson part number SERIAL-MINI-D2 converts this to a standard male DB9 interface.

To remove the board from the chassis, reverse the procedure and press the red locking tabs (IEEE handles only) to extract the board.

## 2.7 Completing the Installation

The MVME8100 is designed to operate as an application-specific compute blade or an intelligent I/O board/carrier. It can be used in any slot in a VME chassis. When the MVME8100 is installed in a chassis, you are ready to connect peripherals and apply power to the board.

Figure 3-1 on page 47 show the locations of the various connectors on the MVME8100.

**NOTICE**

Product Damage
RJ-45 connectors on modules are either twisted-pair Ethernet (TPE) or E1/T1/J1 network interfaces. Connecting an E1/T1/J1 line to an Ethernet connector may damage your system.

- Make sure that TPE connectors near your working area are clearly marked as network connectors.
- Verify that the length of an electric cable connected to a TPE bushing does not exceed 100 meters.
- Make sure the TPE bushing of the system is connected only to safety extra low voltage circuits (SELV circuits).

If in doubt, ask your system administrator.

The console settings for the MVME8100 are:

- Eight bits per character
- One stop bit per character
- Parity disabled (no parity)
- Baud rate of 9600 baud

Verify that hardware is installed and the power/peripheral cables connected are appropriate for your system configuration.

Replace the chassis or system cover, reconnect the chassis to the AC or DC power source, and turn the equipment power on.

# Controls, LEDs, and Connectors

## 3.1 Overview

This chapter summarizes the controls, LEDs and connectors for the MVME8100 baseboard.

## 3.2 Front Panel

The following switch, LEDs, and connectors are available on the MVME8100 front panel. Refer to Figure 3-1 for the location of each.

*Figure 3-1 ENP1 Board Front Panel LEDs, Connectors, Switch*

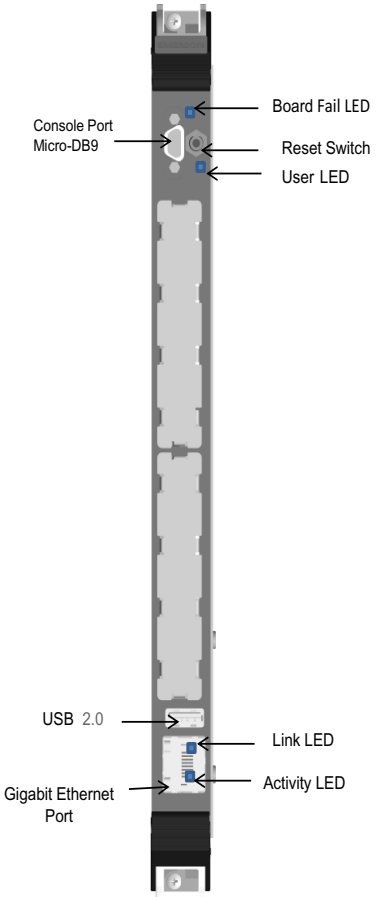
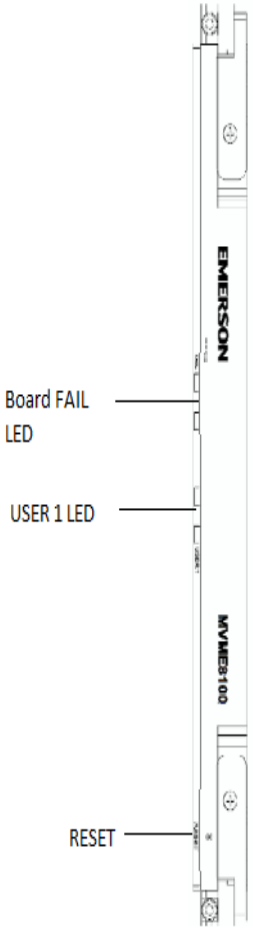


*Figure 3-2 ENP4 Front Panel LEDs*



## 3.2.1 LEDS

### 3.2.1.1 Front Panel LEDs

Table 3-1 describes the LEDs on the front panel of the MVME8100. Refer to Figure 3-1 for LED locations.

*Table 3-1 Front Panel LEDs*

| Label | Function | Color | Description |
|---|---|---|---|
| USER 1 | User Defined | Off | By Default |
| | | Yellow | User Software Controllable. |
| | | Red | User Software Controllable. |
| FAIL | Board Fail | Off | Normal operation after successful firmware boot |
| | | Red | One or more on-board power rails have failed and the board has shutdown to protect the hardware. Normal during power up, during hardware reset (such as a front panel reset). May be asserted by the BDFAIL bit in the Tsi148 VSTAT register |
| SPEED | Link/Speed | Off | No link |
| | | Amber | 10/100BASE-T operation |
| | | Green | 1000 BASE-T operation |
| ACT | Activity | Off | No activity |
| | | Blinking Green | Activity proportional to bandwidth utilization |

## 3.2.2 Connectors

This section describes the pin assignments and signals for the connectors on the MVME8100.

### 3.2.2.1 External Connectors

#### 3.2.2.1.1 Front Panel Connectors

The following are the Front Panel Connectors:

- Serial Console Port (J1)
- Front Panel Ethernet Connector (J1)
- USB Connector (J5)

*Table 3-2 Console Front Panel Connector (J1)*

| PIN No | RS232 SIGNALING | RS485 SIGNALING |
|---|---|---|
| 1 | NC | NC |
| 2 | COM_0_RX | COM_0_RX- |
| 3 | COM_0_TX | COM_0_TX- |
| 4 | NC | NC |
| 5 | GND | GND |
| 6 | NC | NC |
| 7 | COM_0_RTS | COM0_TX+ |
| 8 | COM_0_CTS | COM0_RX+ |
| 9 | NC | NC |

*Table 3-3 Front Panel Tri- Speed Ethernet Connector (J1)*

| Pin No | Signal Description |
|---|---|
| 1 | TD0+ |
| 2 | TD0- |
| 3 | TD1+ |
| 4 | TD2+ |

*Table 3-3 Front Panel Tri- Speed Ethernet Connector (J1)*

| Pin No | Signal Description |
|---|---|
| 5 | TD2- |
| 6 | TD1- |
| 7 | TD3+ |
| 8 | TD3- |

*Table 3-4 USB Connector (J5)*

| Pin No | Signal Description |
|---|---|
| 1 | +5V |
| 2 | Data - |
| 3 | Data + |
| 4 | GND |

### 3.2.2.1.2 Backplane Connectors

*Table 3-5 P1 Connectors*

| P1 Connector (1st Row) | | P1 Connector (2nd Row) | | P1 Connector (3rd Row) | | P1 Connector (4th Row) | | P1 Connector (5th Row) | |
|---|---|---|---|---|---|---|---|---|---|
| Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description |
| A1 | DATA 0 | B1 | BBSY | C1 | DATA 8 | D1 | +5V | Z1 | NC |
| A2 | DATA 1 | B2 | BCLR | C2 | DATA 9 | D2 | GND | Z2 | GND |
| A3 | DATA 2 | B3 | ACFAIL | C3 | DATA 10 | D3 | NC | Z3 | NC |
| A4 | DATA 3 | B4 | BGIN0 | C4 | DATA 11 | D4 | NC | Z4 | GND |
| A5 | DATA 4 | B5 | BGOUT0 | C5 | DATA 12 | D5 | NC | Z5 | NC |
| A6 | DATA 5 | B6 | BGIN1 | C6 | DATA 13 | D6 | NC | Z6 | GND |
| A7 | DATA 6 | B7 | BGOUT1 | C7 | DATA 14 | D7 | NC | Z7 | NC |

*Table 3-5 P1 Connectors*

| P1 Connector (1st Row) | | P1 Connector (2nd Row) | | P1 Connector (3rd Row) | | P1 Connector (4th Row) | | P1 Connector (5th Row) | |
|---|---|---|---|---|---|---|---|---|---|
| Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description |
| A8 | DATA 7 | B8 | BGIN2 | C8 | DATA 15 | D8 | NC | Z8 | GND |
| A9 | GND | B9 | BGOUT2 | C9 | GND | D9 | GAP | Z9 | NC |
| A10 | SYSCLK | B10 | BGIN3 | C10 | SYSFAIL | D10 | GA0 | Z10 | GND |
| A11 | GND | B11 | BGOUT3 | C11 | BERR | D11 | GA1 | Z11 | NC |
| A12 | DS1 | B12 | BR0 | C12 | SYSRESET | D12 | +3.3V (not used) | Z12 | GND |
| A13 | DS0 | B13 | BR1 | C13 | LWORD | D13 | GA2 | Z13 | NC |
| A14 | WRITE | B14 | BR2 | C14 | AM 5 | D14 | +3.3V (not used) | Z14 | GND |
| A15 | GND | B15 | BR3 | C15 | ADD 23 | D15 | GA3 | Z15 | NC |
| A16 | DTACK | B16 | AM 0 | C16 | ADD 22 | D16 | +3.3V (not used) | Z16 | GND |
| A17 | GND | B17 | AM 1 | C17 | ADD 21 | D17 | GA4 | Z17 | NC |
| A18 | AS | B18 | AM 2 | C18 | ADD 20 | D18 | +3.3V (not used) | Z18 | GND |
| A19 | GND | B19 | AM 3 | C19 | ADD 19 | D19 | NC | Z19 | NC |
| A20 | IACK | B20 | GND | C20 | ADD 18 | D20 | +3.3V (not used) | Z20 | GND |
| A21 | IACKIN | B21 | NC | C21 | ADD 17 | D21 | NC | Z21 | NC |
| A22 | IACKOUT | B22 | NC | C22 | ADD 16 | D22 | +3.3V (not used) | Z22 | GND |
| A23 | AM 4 | B23 | GND | C23 | ADD 15 | D23 | NC | Z23 | NC |
| A24 | ADD 7 | B24 | IRQ7 | C24 | ADD 14 | D24 | +3.3V (not used) | Z24 | GND |
| A25 | ADD 6 | B25 | IRQ6 | C25 | ADD 13 | D25 | NC | Z25 | NC |
| A26 | ADD 5 | B26 | IRQ5 | C26 | ADD 12 | D26 | +3.3V (not used) | Z26 | GND |

*Table 3-5 P1 Connectors*

| P1 Connector (1st Row) | | P1 Connector (2nd Row) | | P1 Connector (3rd Row) | | P1 Connector (4th Row) | | P1 Connector (5th Row) | |
|---|---|---|---|---|---|---|---|---|---|
| Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description |
| A27 | ADD 4 | B27 | IRQ4 | C27 | ADD 11 | D27 | NC | Z27 | NC |
| A28 | ADD 3 | B28 | IRQ3 | C28 | ADD 10 | D28 | +3.3V (not used) | Z28 | GND |
| A29 | ADD 2 | B29 | IRQ2 | C29 | ADD 9 | D29 | NC | Z29 | NC |
| A30 | ADD 1 | B30 | IRQ1 | C30 | ADD 8 | D30 | +3.3V (not used) | Z30 | GND |
| A31 | -12V | B31 | NC | C31 | +12V | D31 | GND | Z31 | NC |
| A32 | +5V | B32 | +5V | C32 | +5V | D32 | +5V | Z32 | GND |

*Table 3-6 P2 Connectors*

| P2 Connector (1st Row) | | P2 Connector (2nd Row) | | P2 Connector (3rd Row | | P2 Connector (4th Row) | | P2 Connector (5th Row) | |
|---|---|---|---|---|---|---|---|---|---|
| Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description |
| A1 | PMC IO 2 | B1 | +5V | C1 | PMC IO 1 | D1 | NC | Z1 | GIGE3_MDIO0_P |
| A2 | PMC IO 4 | B2 | GND | C2 | PMC IO 3 | D2 | NC | Z2 | GND |
| A3 | PMC IO 6 | B3 | RETRY | C3 | PMC IO 5 | D3 | GND | Z3 | GIGE3_MDIO0_N |
| A4 | PMC IO 8 | B4 | ADDRESS 24 | C4 | PMC IO 7 | D4 | USB1_P | Z4 | GND |
| A5 | PMC IO 10 | B5 | ADDRESS 25 | C5 | PMC IO 9 | D5 | USB1_N | Z5 | GIGE3_MDIO1_P |
| A6 | PMC IO 12 | B6 | ADDRESS 26 | C6 | PMC IO 11 | D6 | GND | Z6 | GND |
| A7 | PMC IO 14 | B7 | ADDRESS 27 | C7 | PMC IO 13 | D7 | USB2_P | Z7 | GIGE3_MDIO1_N |

*Table 3-6 P2 Connectors*

| P2 Connector (1st Row) | | P2 Connector (2nd Row) | | P2 Connector (3rd Row | | P2 Connector (4th Row) | | P2 Connector (5th Row) | |
|---|---|---|---|---|---|---|---|---|---|
| Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description |
| A8 | PMC IO 16 | B8 | ADDRESS 28 | C8 | PMC IO 15 | D8 | USB2_N | Z8 | GND |
| A9 | PMC IO 18 | B9 | ADDRESS 29 | C9 | PMC IO 17 | D9 | RTM_SIO | Z9 | GIGE3_MDIO2_P |
| A10 | PMC IO 20 | B10 | ADDRESS 30 | C10 | PMC IO 19 | D10 | BPSWITCH_N | Z10 | GND |
| A11 | PMC IO 22 | B11 | ADDRESS 31 | C11 | PMC IO 21 | D11 | GPIO_2 | Z11 | GIGE3_MDIO2_N |
| A12 | PMC IO 24 | B12 | GND | C12 | PMC IO 23 | D12 | GPIO_3 | Z12 | GND |
| A13 | PMC IO 26 | B13 | +5V | C13 | PMC IO 25 | D13 | I2C DATA | Z13 | GIGE3_MDIO3_P |
| A14 | PMC IO 28 | B14 | DATA 16 | C14 | PMC IO 27 | D14 | I2C CLK | Z14 | GND |
| A15 | PMC IO 30 | B15 | DATA 17 | C15 | PMC IO 29 | D15 | COM1_RX/COM1_RX_N | Z15 | GIGE3_MDIO3_N |
| A16 | PMC IO 32 | B16 | DATA 18 | C16 | PMC IO 31 | D16 | COM1_CTS_N/COM1_RX_P | Z16 | GND |
| A17 | PMC IO 34 | B17 | DATA 19 | C17 | PMC IO 33 | D17 | COM2_RX/COM2_RX_N | Z17 | GIGE4_MDIO0_P |
| A18 | PMC IO 36 | B18 | DATA 20 | C18 | PMC IO 35 | D18 | COM2_CTS_N/COM2_RX_P | Z18 | GND |
| A19 | PMC IO 38 | B19 | DATA 21 | C19 | PMC IO 37 | D19 | COM3_RX/COM3_RX_N | Z19 | GIGE4_MDIO0_N |
| A20 | PMC IO 40 | B20 | DATA 22 | C20 | PMC IO 39 | D20 | COM3_CTS_N/COM3_RX_P | Z20 | GND |

*Table 3-6 P2 Connectors*

| P2 Connector (1st Row) | | P2 Connector (2nd Row) | | P2 Connector (3rd Row | | P2 Connector (4th Row) | | P2 Connector (5th Row) | |
|---|---|---|---|---|---|---|---|---|---|
| Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description |
| A21 | PMC IO 42 | B21 | DATA 23 | C21 | PMC IO 41 | D21 | COM4_RX/ COM4_RX_ N | Z21 | GIGE4_MD IO1_P |
| A22 | PMC IO 44 | B22 | GND | C22 | PMC IO 43 | D22 | COM4_CTS _N/COM4_ RX_P | Z22 | GND |
| A23 | PMC IO 46 | B23 | DATA 24 | C23 | PMC IO 45 | D23 | COM1_TX/ COM1_TX_ N | Z23 | GIGE4_MD IO1_N |
| A24 | PMC IO 48 | B24 | DATA 25 | C24 | PMC IO 47 | D24 | COM1_RTS _N/COM1_ TX_P | Z24 | GND |
| A25 | PMC IO 50 | B25 | DATA 26 | C25 | PMC IO 49 | D25 | COM2_TX/ COM2_TX_ N | Z25 | GIGE4_MD IO2_P |
| A26 | PMC IO 52 | B26 | DATA 27 | C26 | PMC IO 51 | D26 | COM2_RTS _N/COM2_ TX_P | Z26 | GND |
| A27 | PMC IO 54 | B27 | DATA 28 | C27 | PMC IO 53 | D27 | COM3_TX/ COM3_TX_ N | Z27 | GIGE4_MD IO2_N |
| A28 | PMC IO 56 | B28 | DATA 29 | C28 | PMC IO 55 | D28 | COM3_RTS _N/COM3_ TX_P | Z28 | GND |
| A29 | PMC IO 58 | B29 | DATA 30 | C29 | PMC IO 57 | D29 | COM4_TX/ COM4_TX_ N | Z29 | GIGE4_MD IO3_P |
| A30 | PMC IO 60 | B30 | DATA 31 | C30 | PMC IO 59 | D30 | COM4_RTS _N/COM4_ TX_P | Z30 | GND |

*Table 3-6 P2 Connectors*

| P2 Connector (1st Row) | | P2 Connector (2nd Row) | | P2 Connector (3rd Row | | P2 Connector (4th Row) | | P2 Connector (5th Row) | |
|---|---|---|---|---|---|---|---|---|---|
| Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description | Pin Name | Signal Description |
| A31 | PMC IO 62 | B31 | GND | C31 | PMC IO 61 | D31 | GND | Z31 | GIGE4_MD IO3_N |
| A32 | PMC IO 64 | B32 | +5V | C32 | PMC IO 63 | D32 | +5V | Z32 | GND |

*Table 3-7 VXS P0 Connector*

| Pin | Row G | Row F | Row E | Row D | Row C | Row B | Row A |
|---|---|---|---|---|---|---|---|
| 1 | NC | GND | P1_TX0_N | P1_TX0_P | GND | P1_RX0_N | P1_RX0_P |
| 2 | GND | P1_TX1_N | P1_TX1_P | GND | P1_RX1_N | P1_RX1_P | GND |
| 3 | NC | GND | P1_TX2_N | P1_TX2_P | GND | P1_RX2_N | P1_RX2_P |
| 4 | GND | P1_TX3_N | P1_TX3_P | GND | P1_RX3_N | P1_RX3_P | GND |
| 5 | NC | GND | SG_TX0_N | SG_TX0_P | GND | SG_RX0_N | SG_RX0_P |
| 6 | GND | NC | NC | GND | NC | NC | GND |
| 7 | GPIO0 | GND | NC | NC | GND | NC | NC |
| 8 | GND | NC | NC | GND | NC | NC | GND |
| 9 | GPIO1 | GND | NC | NC | GND | NC | NC |
| 10 | GND | SATA_TX_N | SATA_TX_P | GND | SATA_RX_N | SATA_RX_P | GND |
| 11 | NC | GND | SG_TX1_N | SG_TX1_P | GND | SG_RX1_N | SG_RX1_P |
| 12 | GND | P2_TX0_N | P2_TX0_N | GND | P2_RX0_N | P2_RX0_P | GND |
| 13 | NC | GND | P2_TX1_N | P2_TX1_P | GND | P2_RX1_N | P2_RX1_P |
| 14 | GND | P2_TX2_N | P2_TX2_P | GND | P2_RX2_N | P2_RX2_P | GND |
| 15 | NC | GND | P2_TX3_N | P2_TX3_P | GND | P2_RX3_N | P2_RX3_P |

### 3.2.2.2 On-board Connectors

The on-board customized SATA connector is compatible with the MVME8100 SATA kit.

Following are the onboard connectors:

- SATA connector
- PMC connector
- Asset JTAG connector
- COP connector
- XMC connector

SATA Connector:

The on-board customized SATA connector is compatible with the Emerson SATA kit MVME8100-HDMNTKIT4.

*Table 3-8 Customized SATA Connector*

| Pin Name | Signal Description | Pin Name | Signal Description |
|---|---|---|---|
| 1 | GND | 21 | GND |
| 2 | GND | 22 | SATA POWER ENABLE |
| 3 | NC | 23 | NC |
| 4 | SATA TX + | 24 | SATA DETECT |
| 5 | NC | 25 | NC |
| 6 | SATA TX - | 26 | GND |
| 7 | GND | 27 | NC |
| 8 | GND | 28 | GND |
| 9 | GND | 29 | GND |
| 10 | GND | 30 | GND |
| 11 | NC | 31 | +3.3V |
| 12 | SATA RX - | 32 | +5V |
| 13 | NC | 33 | +3.3V |
| 14 | SATA RX + | 34 | +5V |
| 15 | GND | 35 | +3.3V |
| 16 | GND | 36 | +5V |

*Table 3-8 Customized SATA Connector*

| Pin Name | Signal Description | Pin Name | Signal Description |
|---|---|---|---|
| 17 | NC | 37 | +3.3V |
| 18 | GND | 38 | +5V |
| 19 | NC | 39 | +3.3V |
| 20 | GND | 40 | +5V |

PMC Connectors

The MVME8100 supports two PMC sites. The connector is located on the middle portion of the board. It utilizes J14 to support PMC I/O that goes to RTM PMC.

*Table 3-9 PMC J11/J21 Connector*

| Pin Name | Signal Description | Pin Name | Signal Description |
|---|---|---|---|
| 1 | JTAG TCK | 33 | FRAME |
| 2 | -12V | 34 | GND |
| 3 | GND | 35 | GND |
| 4 | INT A | 36 | IRDY |
| 5 | INT B | 37 | DEVSEL |
| 6 | INT C | 38 | +5V |
| 7 | PRESENT SIGNAL | 39 | PCIXCAP |
| 8 | +5V | 40 | LOCK |
| 9 | INT D | 41 | NC |
| 10 | NC | 42 | NC |
| 11 | GND | 43 | PAR |
| 12 | NC | 44 | GND |
| 13 | PCI CLK | 45 | +3.3V |
| 14 | GND | 46 | AD 15 |
| 15 | GND | 47 | AD 12 |
| 16 | GNT A | 48 | AD 11 |

*Table 3-9 PMC J11/J21 Connector*

| Pin Name | Signal Description | Pin Name | Signal Description |
|---|---|---|---|
| 17 | REQ A | 49 | AD 9 |
| 18 | +5V | 50 | +5V |
| 19 | +3.3V | 51 | GND |
| 20 | AD 31 | 52 | CBE0 |
| 21 | AD 28 | 53 | AD 6 |
| 22 | AD 27 | 54 | AD 5 |
| 23 | AD 25 | 55 | AD 4 |
| 24 | GND | 56 | GND |
| 25 | GND | 57 | +3.3V |
| 26 | CBE3 | 58 | AD 3 |
| 27 | AD 22 | 59 | AD 2 |
| 28 | AD 21 | 60 | AD 1 |
| 29 | AD 19 | 61 | AD 0 |
| 30 | +5V | 62 | +5V |
| 31 | +3.3V | 63 | GND |
| 32 | AD 17 | 64 | REQ64 |

*Table 3-10 PMC J12/J22 Connector*

| Pin Name | Signal Description | Pin Name | Signal Description |
|---|---|---|---|
| 1 | +12V | 33 | GND |
| 2 | JTAG TRST | 34 | IDSELB |
| 3 | JTAG TMS | 35 | TRDY |
| 4 | JTAG TDO | 36 | +3.3V |
| 5 | JTAG TDI | 37 | GND |
| 6 | GND | 38 | STOP |
| 7 | GND | 39 | PERR |
| 8 | NC | 40 | GND |

*Table 3-10 PMC J12/J22 Connector*

| Pin Name | Signal Description | Pin Name | Signal Description |
|---|---|---|---|
| 9 | NC | 41 | +3.3V |
| 10 | NC | 42 | SERR |
| 11 | BUSMODE2 (Pulled UP) | 43 | CBE1 |
| 12 | +3.3V | 44 | GND |
| 13 | PCI RESET | 45 | AD 14 |
| 14 | BUSMODE3 (PULLED DWN) | 46 | AD 13 |
| 15 | +3.3V | 47 | M66EN |
| 16 | BUSMODE4 (PULLED DWN) | 48 | AD 10 |
| 17 | NC | 49 | AD 8 |
| 18 | GND | 50 | +3.3V |
| 19 | AD 30 | 51 | AD 7 |
| 20 | AD 29 | 52 | REQB |
| 21 | GND | 53 | +3.3V |
| 22 | AD 26 | 54 | GNTB |
| 23 | AD 24 | 55 | NC |
| 24 | +3.3V | 56 | GND |
| 25 | IDSEL | 57 | NC |
| 26 | AD 23 | 58 | EREADY |
| 27 | +3.3V | 59 | GND |
| 28 | AD 28 | 60 | RSTOUT |
| 29 | AD 18 | 61 | ACK64 |
| 30 | GND | 62 | +3.3V |
| 31 | AD 16 | 63 | GND |
| 32 | CBE2 | 64 | NC |

*Table 3-11 PMC J13/J23 Connectors*

| Pin Name | Signal Description | Pin Name | Signal Description |
|---|---|---|---|
| 1 | NC | 33 | GND |
| 2 | GND | 34 | AD48 |
| 3 | GND | 35 | AD 47 |
| 4 | CBE7 | 36 | AD 52 |
| 5 | CBE6 | 37 | AD 45 |
| 6 | CBE5 | 38 | GND |
| 7 | CBE4 | 39 | +3.3V |
| 8 | GND | 40 | AD 40 |
| 9 | +3.3V | 41 | AD 43 |
| 10 | PAR64 | 42 | AD 42 |
| 11 | +3.3V | 43 | AD 41 |
| 12 | AD 62 | 44 | GND |
| 13 | AD 61 | 45 | GND |
| 14 | GND | 46 | AD 40 |
| 15 | GND | 47 | AD 39 |
| 16 | AD 60 | 48 | AD 38 |
| 17 | AD 59 | 49 | AD 37 |
| 18 | AD 58 | 50 | GND |
| 19 | AD 57 | 51 | GND |
| 20 | GND | 52 | AD 36 |
| 21 | +3.3V | 53 | AD 35 |
| 22 | AD 56 | 54 | AD 34 |
| 23 | AD 55 | 55 | AD 33 |
| 24 | AD 54 | 56 | GND |
| 25 | AD 53 | 57 | +3.3V |
| 26 | GND | 58 | AD 32 |
| 27 | GND | 59 | NC |

*Table 3-11 PMC J13/J23 Connectors*

| Pin Name | Signal Description | Pin Name | Signal Description |
|---|---|---|---|
| 28 | GND | 60 | NC |
| 29 | AD 51 | 61 | NC |
| 30 | AD 50 | 62 | GND |
| 31 | AD 49 | 63 | GND |
| 32 | GND | 64 | NC |

*Table 3-12 PMC J14 Connector*

| Pin Name | Signal Description | Pin Name | Signal Description |
|---|---|---|---|
| 1 | PMC IO 1 | 33 | PMC IO 33 |
| 2 | PMC IO 2 | 34 | PMC IO 34 |
| 3 | PMC IO 3 | 35 | PMC IO 35 |
| 4 | PMC IO 4 | 36 | PMC IO 36 |
| 5 | PMC IO 5 | 37 | PMC IO 37 |
| 6 | PMC IO 6 | 38 | PMC IO 38 |
| 7 | PMC IO 7 | 39 | PMC IO 39 |
| 8 | PMC IO 8 | 40 | PMC IO 40 |
| 9 | PMC IO 9 | 41 | PMC IO 41 |
| 10 | PMC IO 10 | 42 | PMC IO 42 |
| 11 | PMC IO 11 | 43 | PMC IO 43 |
| 12 | PMC IO 12 | 44 | PMC IO 44 |
| 13 | PMC IO 13 | 45 | PMC IO 45 |
| 14 | PMC IO 14 | 46 | PMC IO 46 |
| 15 | PMC IO 15 | 47 | PMC IO 47 |
| 16 | PMC IO 16 | 48 | PMC IO 48 |
| 17 | PMC IO 17 | 49 | PMC IO 49 |
| 18 | PMC IO 18 | 50 | PMC IO 50 |
| 19 | PMC IO 19 | 51 | PMC IO 51 |

*Table 3-12 PMC J14 Connector*

| | | | |
|---|---|---|---|
| 20 | PMC IO 20 | 52 | PMC IO 52 |
| 21 | PMC IO 21 | 53 | PMC IO 53 |
| 22 | PMC IO 22 | 54 | PMC IO 54 |
| 23 | PMC IO 23 | 55 | PMC IO 55 |
| 24 | PMC IO 24 | 56 | PMC IO 56 |
| 25 | PMC IO 25 | 57 | PMC IO 57 |
| 26 | PMC IO 26 | 58 | PMC IO 58 |
| 27 | PMC IO 27 | 59 | PMC IO 59 |
| 28 | PMC IO 28 | 60 | PMC IO 60 |
| 29 | PMC IO 29 | 61 | PMC IO 61 |
| 30 | PMC IO 30 | 62 | PMC IO 62 |
| 31 | PMC IO 31 | 63 | PMC IO 63 |
| 32 | PMC IO 32 | 64 | PMC IO 64 |

Asset JTAG Connector

The MVME8100 contains a 20-pin 0.1" header for an Asset JTAG header. The pinout for the header is given in the following table.

*Table 3-13 Asset JTAG Header Pin Assignment*

| PIN Number | Description | PIN Number | Description |
|---|---|---|---|
| 1 | TCK | 2 | ASSET_PRSNT_L (GND on cable) |
| 3 | TDO | 4 | GND |
| 5 | TMS | 6 | GND |
| 7 | TRST_L | 8 | GND |
| 9 | TDI | 10 | GND |
| 11 | No Pin Key | 12 | Reserved - NC |
| 13 | GND | 14 | Reserved - NC |
| 15 | GND | 16 | Reserved - NC |

*Table 3-13 Asset JTAG Header Pin Assignment*

| PIN Number | Description | PIN Number | Description |
|---|---|---|---|
| 17 | GND | 18 | Reserved - NC |
| 19 | GND | 20 | Reserved - NC |

XMC Connector

MVME8100 supports two XMC sites. The board only supports J15 for XMC site 1 and J25 for XMC site 2.

*Table 3-14 XMC Connectors*

| XJ1/2 (ROW A) | | XJ1/2 (ROW B) | | XJ1/2 (ROW C) | | XJ1/2 (ROW D) | | XJ1/2 (ROW E) | | XJ1/2 (ROW F) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin No | Signal Description | Pin No | Signal Description | Pin No | Signal Description | Pin No | Signal Description | Pin No | Signal Description | Pin No | Signal Description |
| 1 | RX0 + | 1 | RX0 - | 1 | +3.3V | 1 | RX0 + | 1 | RX1 - | 1 | +3.3V |
| 2 | GND | 2 | GND | 2 | JTAG TRST | 2 | GND | 2 | GND | 2 | HRESET |
| 3 | NC | 3 | NC | 3 | +3.3V | 3 | NC | 3 | NC | 3 | +3.3V |
| 4 | GND | 4 | GND | 4 | JTAG TCK | 4 | GND | 4 | GND | 4 | MRSTO (PULLED UP) |
| 5 | NC | 5 | NC | 5 | +3.3V | 5 | NC | 5 | NC | 5 | +3.3V |
| 6 | GND | 6 | GND | 6 | JTAG TMS | 6 | GND | 6 | GND | 6 | +12V |
| 7 | NC | 7 | NC | 7 | +3.3V | 7 | NC | 7 | NC | 7 | +3.3V |
| 8 | GND | 8 | GND | 8 | JTAG TMS | 8 | GND | 8 | GND | 8 | -12V |
| 9 | NC | 9 | NC | 9 | NC | 9 | NC | 9 | NC | 9 | +3.3V |
| 10 | GND | 10 | GND | 10 | JTAG TDO | 10 | GND | 10 | GND | 10 | GA 0 |
| 11 | TX0 | 11 | TX0 - | 11 | BIST (PULLED UP) | 11 | TX1 + | 11 | TX1 - | 11 | +3.3V |
| 12 | GND | 12 | GND | 12 | GA 1 | 12 | GND | 12 | GND | 12 | PRESENT |
| 13 | NC | 13 | NC | 13 | NC | 13 | NC | 13 | NC | 13 | +3.3V |
| 14 | GND | 14 | GND | 14 | GA 2 | 14 | GND | 14 | GND | 14 | I2C DATA |
| 15 | NC | 15 | NC | 15 | NC | 15 | NC | 15 | NC | 15 | +3.3V |

*Table 3-14 XMC Connectors*

| XJ1/2 (ROW A) | | XJ1/2 (ROW B) | | XJ1/2 (ROW C) | | XJ1/2 (ROW D) | | XJ1/2 (ROW E) | | XJ1/2 (ROW F) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin No | Signal Description | Pin No | Signal Description | Pin No | Signal Description | Pin No | Signal Description | Pin No | Signal Description | Pin No | Signal Description |
| 16 | GND | 16 | GND | 16 | MVMRO (PULLED DOWN) | 16 | GND | 16 | GND | 16 | I2C CLOCK |
| 17 | NC | 17 | NC | 17 | NC | 17 | NC | 17 | NC | 17 | NC |
| 18 | GND | 18 | GND | 18 | NC | 18 | GND | 18 | GND | 18 | NC |
| 19 | CLK + | 19 | CLK - | 19 | NC | 19 | NC | 19 | ROOT0 (PULLED UP) | 19 | NC |

# Functional Description

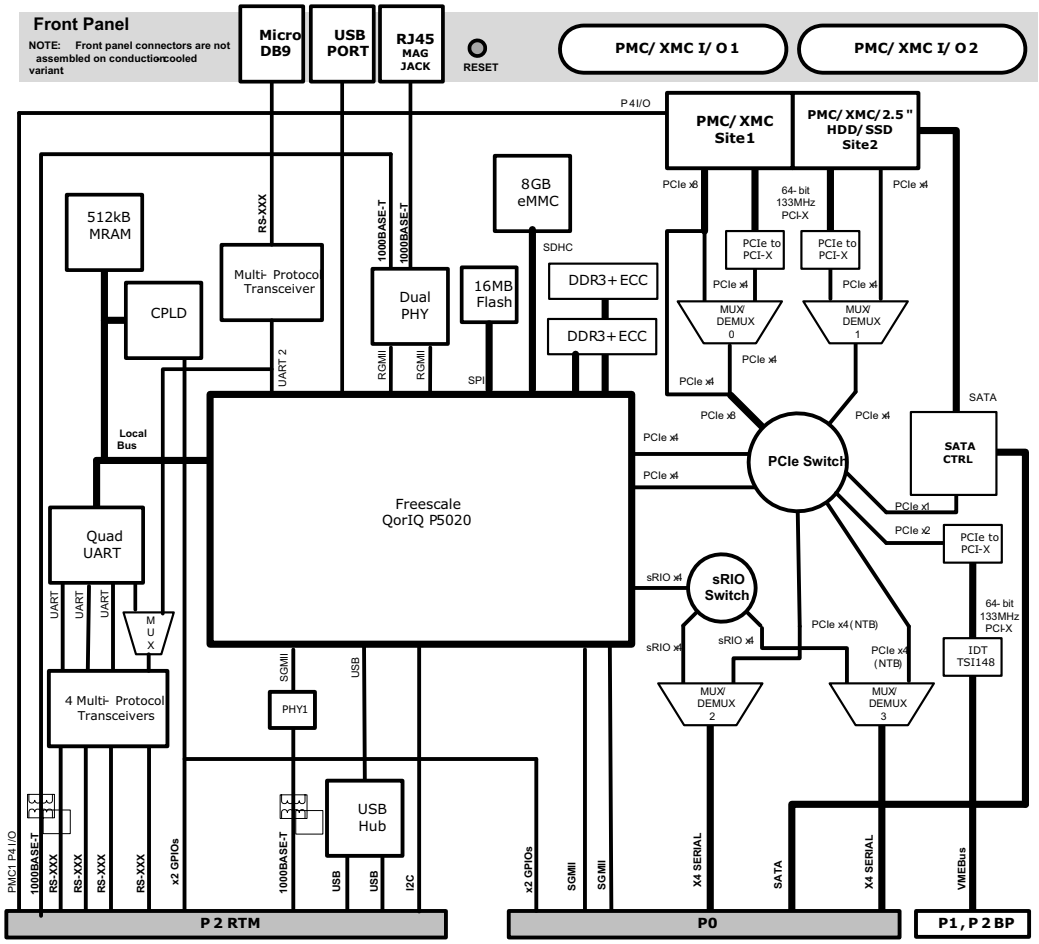
## 4.1 Overview

The MVME8100 Single Board Computer is a 6U VME/VXS board based on the Freescale QorIQ P5020 processor. This section describes the features of MVME8100.

# 4.2 Block Diagram

Figure 4-1 illustrates the MVME8100 architecture.

*Figure 4-1 Block Diagram*



## 4.3 Processor

The P5020 QorIQ processor combines two Power architecture processor cores with high-performance data path acceleration logic and network, and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure and aerospace applications.

This device can be used for combined control, data path and application layer processing in routers, switches, base station controllers, and general-purpose embedded computing. Its high level of integration offers significant performance benefits compared to multiple discrete devices while also greatly simplifies the board design.

The MVME8100 board ENP1 version is designed to use the 2.0 GHz core processor version while the ENP4 version uses the 1.8 GHz processor.

For more information, refer P5020 QorIQ Integrated Multicore Communications Processor Family Reference Manual.

## 4.4 System Memory

The MVME8100 supports four GB DDR3 ECC memory using two banks of 2Gb memory devices.

The memory devices are soldered-down and not modular solution using DIMM sockets. The supported data rate is 1333MT/s. The memory is evenly-distributed across both memory channels (e.g. memory-capacity requirement is 4GB, place 2GB of memory on each channel).

## 4.5 Timers

This section describes the timer functions implemented on MVME8100.

### 4.5.1 Real Time Clock

The MVME8100 implements an Real Time Clock (RTC) to maintain seconds, minutes, hours, day, date, month, and year accurately. It includes a 32.768 KHZ crystal, DS1337 RTC, and back up power. For the ENP1 version of the MVME8100, a battery is used for the RTC back up power. For the ENP4 version, a 3.3V regulator powered from the VME backplane +5V_STDBY voltage is used for back up power. The DS1337 has an interrupt output (INTA) which can be programmed to assert a processor IRQ on a time/day/date match. The DS1337 also has a 32.768 KHz clock output (SQW) which is used to drive the P5020 RTC input signal.

The RTC internal oscillator has been disabled before the board was shipped from the factory. Use the following process to turn on the RTC oscillator from Uboot:

```
MVME8100 => i2c mm 0x68 e.1
0000000e: 98 ? 18
0000000f: 80 ? n
```

To set the date, use the following uboot command:

```
MVME8100 =>date [MMDDhhmm[[CC]YY][.ss]]
```

### 4.5.2 P5020 Internal Timers

The P5020 provides a total of eight global timers; it is divided into two groups, group A and group B. Each group has four timers. Each timer has four individual configuration register. However, these two groups of timers cannot be cascaded together.

### 4.5.3 Watchdog Timers

The CPLD has two watchdogs timers, the Initial Hardware Watchdog (IWD) and the OS Watchdog (OSWD).

The Initial Hardware Watchdog is used to guard loading of U-Boot and to prevent board hanging up. U-Boot has to service IWD before timeout, or IWD will request Power-On Reset. Following a board reset, the board will try to boot from the U-Boot Flash selected by the configuration switches. If IWD is not serviced in time by U-Boot, then following the IWD reset, the board will attempt to boot from the alternate SPI1 U-Boot Flash device.

The OS Watchdog (OSWD) is used to guard loading of the operating system. The OS has to service OSWD before timeout or OSWD will request a hard reset sequence to reset the board.

If IWD is not serviced after switching over to the SPI1 U-Boot Flash, board will infinitely try to boot to SPI1 U-Boot Flash.

By default, U-Boot will disable both the IWD and the OSWD.

The configuration switch S2-1 is used to enable or disable both watchdogs. By default, the watchdogs are disabled.

#### 4.5.3.1 Initial Hardware Watchdog

Initial Hardware Watchdog (IWD) starts after reset deassertion. This watchdog has to be serviced within 8s after a reset deassertion, otherwise a IWD reset will be requested.

The Initial Hardware Watchdog is serviced by writing 0xEEA1 to CPLD Command/Status Register.

#### 4.5.3.2 OS Watchdog

The OS Watchdog (OSWD) is not armed after reset. It is enabled right after the IWD is disabled. The OSWD timeout is set to 108s. If the timer terminates, the OSWD reset sequence will be initiated.

OSWD is serviced and disabled by writing 0xBBC2 to CPLD Command/Status Register.

### 4.5.4 CPLD Tick Timer

The MVME8100 is designed to provide three independent 32-bit timers. These timers are implemented in the CPLD which provides the fully programmable registers required for these timers.

## 4.6 Ethernet Interfaces

The P5020 has five dTSEC controllers. The controllers can be configured to implement RGMII, GMII, or SGMII interfaces to external Ethernet transceivers.

The MVME8100 utilizes dTSEC4 for a dedicated front panel 10/100/1000BASE-T interface and dTSEC5 for a 10/100/1000BASE-T interface to the RTM via P2. A Broadcom BCM5482 dual transceiver provides the RGMII -> 10/100/1000BASE-T interfaces. A second 10/100/1000BASE-T interface to the RTM through P2 is provided using dTSEC3 in SGMII mode. A Broadcom BCM54616S transceiver provides the SGMII -> 10/100/1000BASE-T interface. The registers of these transceivers can be accessed via the P5020's two-wire Ethernet Management interface.

The front panel RJ45 connector has integrated speed and activity status indicator LED's. Similar to the front panel Ethernet, the RJ45 connectors found in the RTM have integrated speed and activity status indicator LED's. Isolation transformers are provided on-board for each of the RTM ports.

The MVME8100 utilizes dTSEC1 and dTSEC2 in SGMII mode for two additional 1000Base-BX Ethernet ports to P0.

## 4.7 SPI Interface

Firmware boot Flash resides on the P5020 eSPI bus interface.

### 4.7.1 SPI Flash Memory

The P5020 contains two Eight MB serial flash devices. These devices contain the 512 bits of the Reset Configuration Word, the boot firmware image (U-boot), and the ENV environment variables.

### 4.7.2 Firmware Redundancy

The MVME8100 utilizes two separate Eight MB boot devices in order to provide boot firmware redundancy. The P5020 SPI device controller uses Chip Select 0 as the boot device, so CPLD logic is used on the MVME8100 in order to swap the chip select to the boot devices. The chip select control is based upon the configuration switch S5-1.

At power-up, the selection of the SPI boot device is strictly based upon the switch S5-1 setting. The selected SPI device must contain a boot image. The MVME8100 supports automatic SPI FLASH fail-over. If booting on one device is not successful, then the watchdog will trigger a board reset and the CPLD logic automatically toggle chip selects, and tries to boot on the other device.

## 4.8 MRAM

The MVME8100 includes one MR2A16AVYS35 512 KB MRAM device to provide a non-volatile memory, that has virtually unlimited writes (100 trillion), fast access and ten years data retention without power. The MRAM is organized as 256Kx16 and accessible through the P5020 local bus.

## 4.9 eMMC

The MVME8100 contains a soldered down 8GB eMMC device connected to the P5020 eSDHC interface. The eSDHC interface operates in four bit MMC mode and supports up to 200Mbps data transfer for MMC card using four parallel data lines.

## 4.10 Processor Console Port

The MVME8100 utilizes P5020 UART1 port for the processor console interface. This console interface can be routed to the front panel or the P2 connector using configuration switches. The front panel port can be configured for RS-232 or RS-422/RS-485 modes. RS-232 mode supports RX, TX, RTS and CTS signals. Only four wire full duplex RX/TX is supported in RS422/485 mode. The signaling mode is selected through on board configuration switches. The default baud rate on the front panel serial is 9600 baud.

The physical front panel console connector is a male micro-min DB-9. A male- to -male micro-mini DB9 to DB9 adapter cable is available under Emerson Part Number SERIAL MINI-D (30-W2400E01A).

## 4.11 Rear UART Ports

The MVME8100 provides four asynchronous serial UART interfaces to the P2 RTM connector by utilizing Exar's ST16C554 quad UART. The QUART features 16 bytes of transmit and receive FIFO's, it has a selectable receive FIFO trigger levels and data rates of up to 1.5Mbps. Each UART has a set of registers that provide the user with operating status and control. The QUART is a 8 bit device connected to the P5020 through the local bus controller. QUART port A is multiplexed with the P5020 UART1 console port, so that the console port can be routed to the RTM COM1 port. The mux is controlled using configuration switches on S2.

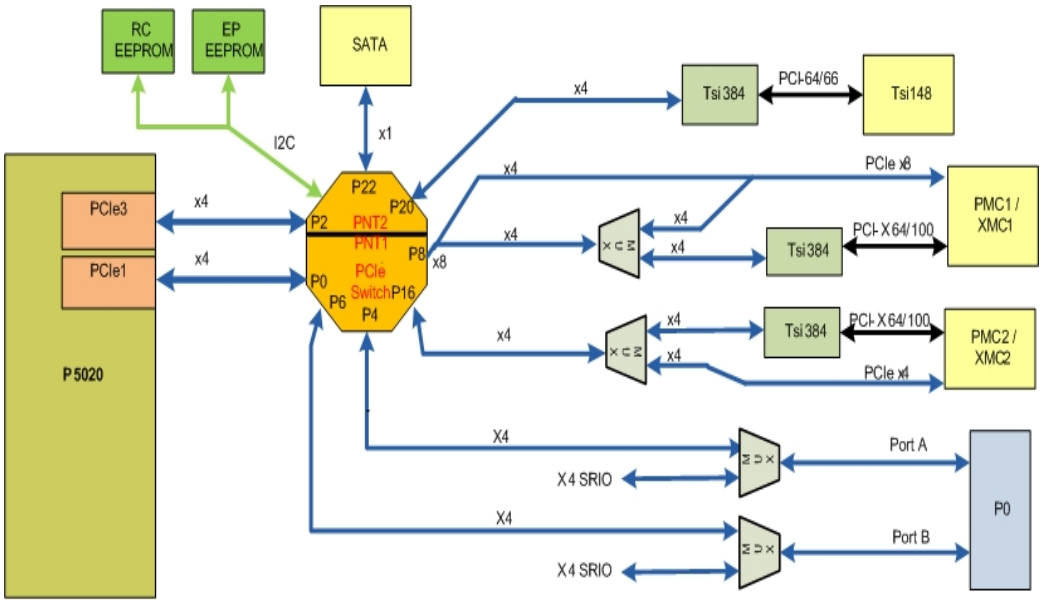
The four ports can be configured for RS-232 or RS-422/RS-485 modes. RS-232 mode supports RX, TX, RTS and CTS signals. Only four wire full duplex RX/TX is supported in RS422/485 mode. The signaling mode is selected through on board configuration switches on S2.

## 4.12 PCIe Ports

The MVME8100 provides multiple PCI Express ports. The P5020 is configured to use two x4 PCIe controllers (#1 and #3) on the MVME8100. Both controllers are configured to operate at Gen 1 data rate (2.5 Gbaud). These ports are routed to an IDT 32NT24AG2 PCIe switch for expansion of the PCIe ports. The IDT switch is a 32 lane Gen 2 device and can support up to 24 ports, 8 of which are capable of NT function. Each port of the switch is configured to operate at Gen 1 data rate. The configuration of the ports and the partitioning of the switch into a single or multiple domains is controlled by an I2C eeprom connected to the PCIe switch master SMbus and loaded into the switch following reset.

The board provides two separate eeproms so that separate configuration data can be maintained for the MVME8100 operating as a root complex or as an end point on the P0 connector ports. The selection of the root complex or end point eeprom for loading the configuration data after reset is determined by the root complex configuration switch S4-2 (see *S4 Switch* on page 36.). The eeproms can be reprogrammed from the processor using the I2C master interface in the IDT device. A swap bit in CPLD control register can be used to temporarily swap the eeprom device addressing so that the alternate eeprom can be reprogrammed. A diagram of the PCIe port configuration is shown in the figure below.

*Figure 4-2 PCIe Ports*



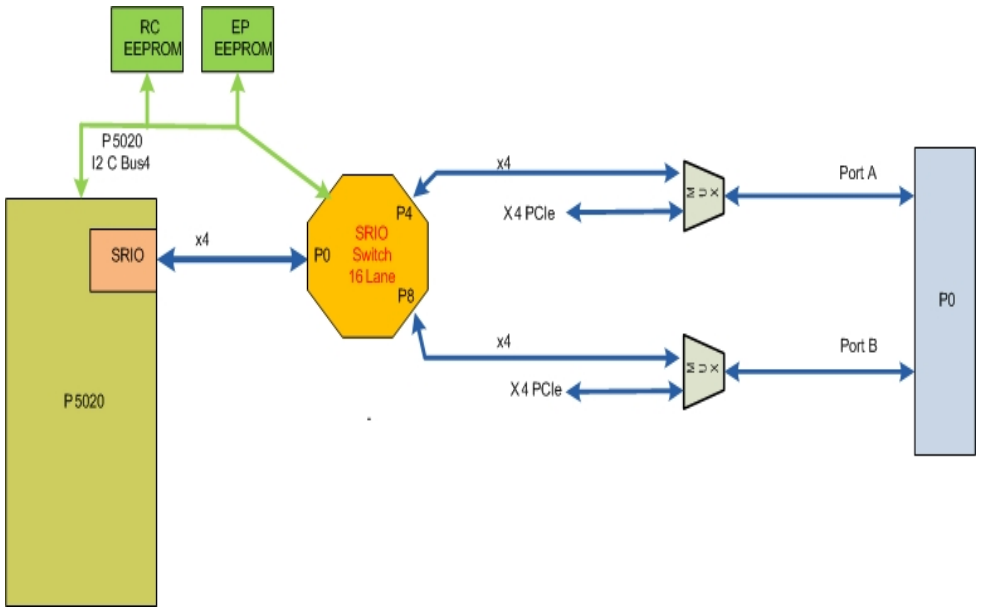

# 4.13 SRIO Ports

The MVME8100 also provides multiple SRIO ports. The P5020 provides a single x4 SRIO configured for 2.5 GBaud data rate. This port is routed to an IDT 80HCPS1616 SRIO switch for expansion of the SRIO ports. The SRIO switch supports multiple lane speeds including 1.25, 2.5, 3.125 and 5.0 Gbaud. The MVME8100 provides two x4 SRIO ports which may be routed to the P0 connector through a high speed mux. The selection of SRIO or PCIe ports to P0 is controlled by the S2-8 configuration switch (see *S2 Switch* on page 33). The configuration of the SRIO switch ports is controlled by an I2C eeprom connected to the SRIO switch I2C bus and loaded into the switch following reset. The board provides two separate eeproms so that separate configuration data can be maintained for the MVME8100 operating as a root complex or as an end point on the P0 ports. The selection of the root complex or end point eeprom for

loading the configuration data after reset is determined by the root complex configuration switch S4-2 (see *S4 Switch* on page 36). The eeproms can be reprogrammed over the processor I2C bus 4 interface. The eeprom device addresses are listed in section *I2C Devices* on page 79. A diagram of the SRIO port topology is shown in the figure below.

The 80HCPS1616 SRIO switch does not support auto baud rate discovery. The switch configuration EEPROMs must program the P0 fabric ports to match the SRIO baud rate of the system. The default baud rate for the P0 fabric ports is 2.5 Gbaud.

*Figure 4-3 SRIO Bus Topology*



## 4.14 PMC/XMC Sites

The MVME8100 provides two PMC/XMC sites. Each PMC/XMC site will accept either a PMC or an XMC add-on card. For a given PMC/XMC site, only an XMC or a PMC maybe populated at any given time, as they occupy the same physical space on the PCB. Combination of PMC/XMC cards are not supported by MVME8100. The PMC/XMC1 site provides rear PMC I/O.

The PMC/XMC sites are fully compliant with the following:

- VITA 39 -PCI-X for PMC
- VITA 35-2000 for PMC P4 to VME P2 Connection (PMC/XMC1 site only)
- PCI Rev 2.2 for PCI Local Bus Specification
- PCI-X PT 2.0 for PCI-X Protocol Addendum to the PCI Local Bus Specs
- IEEE Standard P1386-2001 for Standard for Common Mezzanine Card Family
- IEEE Standard P1386.1-2001 for Standard Physical and Environmental Layer for PCI Mezzanine Card.
- VITA 42 for XMC
- VITA 42.3, PCIe for XMC

PMC/XMC sites are keyed for 3.3V PMC signaling.

MVME8100 provides a x8 PCI Express interface link for PMC/XMC1 and x4 PCI Express interface link for PMC/XMC2. It is designed such that same PCI Express interface is used for either the XMC or the PCIe to PCI-X bridge required for a PMC. This is made possible by using Pericom PI3PCIE3412 PCIe mux devices. The PCIe Mux at both sites is controlled by the CPLD. The CPLD detects the presence signal provided by the XMC or PMC board and it will be used to configure the routing of PCIe Mux accordingly.

### 4.14.1 PMC Add-on Card

The MVME8100 supports up to two PMC cards. PCI-X operation to each site is provided using a separate IDT TSI384 PCIe to PCI-X bridge for each site. Each Tsi384 can support up to 8.5Gbps (64bits x 133 Mhz). An onboard switch will configure the TSI384 to run on either 100 MHz or 133 MHz. The default is 133 MHz.

The MVME8100 supports multi-function PMCs and Processor PMC's (PrPMCs). The PCI signaling voltage (VIO) for the site is 3.3V as required by the Tundra Tsi384 and is keyed as such. The power budget allocated to 3.3V is 16.5W (max) for either PMC or PrPMC. The PMC site has two IDSELs, two REQ/GNT pairs, and EREADY to support PrPMC modules as defined by VITA39.

### 4.14.2 XMC Add-on Card

XMC add-on cards are required to operate off of +5V or +12V (from carrier to XMC). The MVME8100 provides +5V to the XMC VPWR (Variable Power) pins. The MVME8100 does not provide +12V to the XMC VPWR pins. Voltage tolerances for VPWR and all carrier supplied voltage (+3.3V, +12V, -12V) are defined by the base XMC standard.

## 4.15 SATA interface

The MVME8100 is designed to support an optional 2.5 inch SATA HDD/SDD in PMC/XMC site 2. The heat frame has mounting holes to support the 2.5" SSD/HDD on board. The connector interface to the MVME8100 board is compatible with the Emerson SATA mounting kit MVME8100-HDMNTKIT4, which contains a SATA adapter board, screws and mounting brackets. The SATA adapter board provides a standard SATA connector to support horizontal mounting of the HDD/SSD.

MVME8100 utilizes Marvell's 88SE9125B1 SATA controller. This is a PCI Express 2.0 to dual SATA 3.0 Host Bus Adapter. It employs the latest SATA PHY technology, operating at 1.5Gbps or 3.0Gbps.

## 4.16 VME Support

The MVME8100 is designed to comply with VME ANSI/VITA 1.5-2003, 2eSST. The MVME8100 supports most of the addressing and data transfer modes defined by the VME64, VME64x and 2eSST specifications. The MVME8100 can operate in System Controller (SCON) mode or in Non-SCON mode. This is determined by on board switch settings on S4.

### 4.16.1 Tsi148 VME Controller

The Tsi148 provides the required VME64, VME64X and 2eSST functions. TI SN74VMEH22501 transceivers buffer the VME signals between Tsi148 and the VME backplane. Refer to the *IDT Tsi148 User's Manual* for additional details and programming information.

### 4.16.2 Tsi384 PCIe to PCI/PCI-X Bridge

The PCIe to PCI/PCI-X Bridge function required to interface to the Tsi148 is provided by the Tundra Tsi384 device. The Tsi384 is responsible for bridging bi-directional traffic between the PCIe switch and the Tundra Tsi148. Per ANSI/VITA 1.5-2003, the theoretical maximum transfer rate for a 6U VME card in 2eSST mode is 320MBps, or 2.62 Gbps.

## 4.17 USB

The P5020 provides two USB 2.0 controllers with integrated PHYs. The MVME8100 routes USB port 1 to the front panel to an upright USB Type A receptacle. The DC power for the front panel USB port is supplied through Micrel's MIC2076 power switch which provides soft, current limiting, over current detection and power enable.

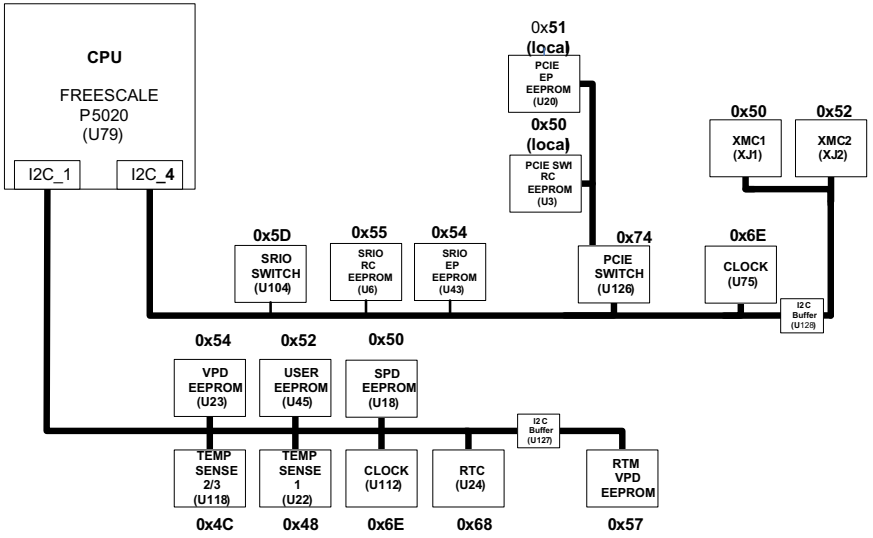
The P5020 USB port 2 is routed to a USB2512 hub device which provides two additional downstream USB 2.0 ports. The two additional downstream ports are routed to the P2 connector for use on the RTM.

## 4.18 I2C Devices

The P5020 provides four I2C controllers, but only controller 1 and controller 4 are used. The I2C ports are connected to multiple devices such as VPD, SPD, User EEPROMs, switch configuration EEPROMs, RTC, temperature sensors, RTM EEPROM, XMC EEPROMS, and clock devices. The RTM and XMC EEPROM addresses are configured such that they do not have an address conflict with other on board device address. The I2C busses and device addresses are shown in Figure

4-4. For more information, refer *MVME8100 Programmer's Reference.*

*Figure 4-4 I2C Busses*




## 4.19 Reset/Control CPLD

The MVME8100 uses a Lattice LCMXO2280C CPLD to provide reset, power up sequencing, timers, miscellaneous board logic, and status/control registers accessible through the P5020 LBC interface. The CPLD uses early 3.3V power from the +5V backplane and can be programmed through JTAG interface pins through the JTAG connector. It uses a 1.8 MHz oscillator for logic control.

The CPLD provides the following functions:

- Power control and fault detection
- Reset sequence and reset management
- Status and Control registers
- Miscellaneous control logics

- Watchdog timer
- 32-bit Tick Timers
- Clock generator
- Switch decoder and LED controller

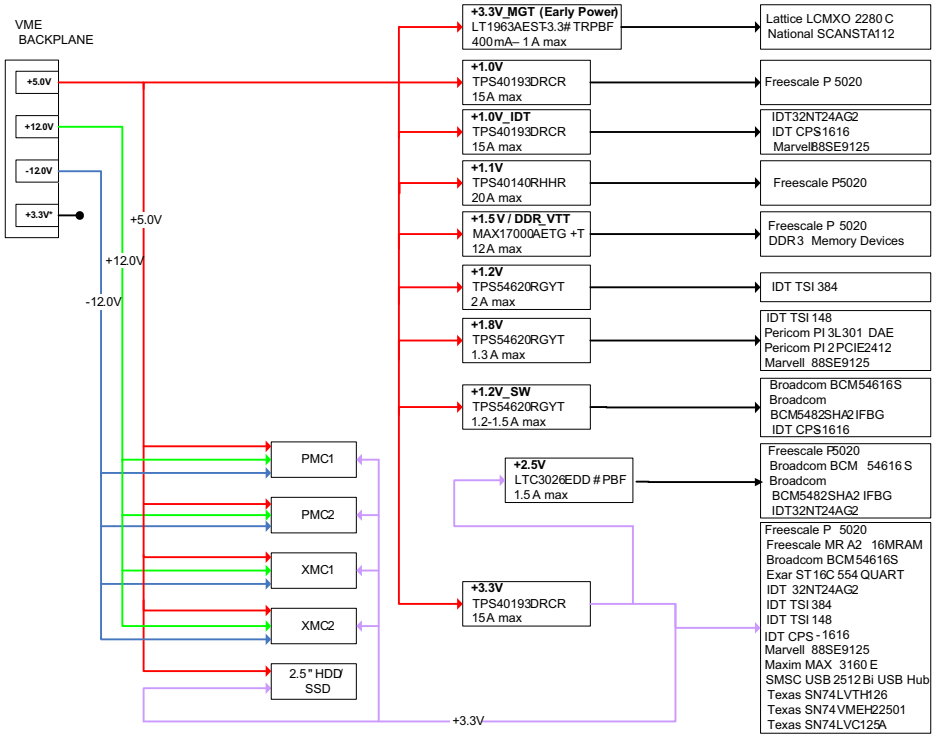
## 4.20 Power Management

The 5 volt coming from the back plane is utilized to derive all on-board voltage rails. To provide the required voltage sequencing, each voltage rail is controlled by the CPLD through enable pin of each regulator and the output is being monitored by CPLD through each regulator power good signal. If one voltage rail fails, the CPLD will disable all of the regulators and the only way to restart the board is by power cycling the chassis 5 volt power.

## 4.20.1 Power Distribution Structure

Figure 4-5 displays the MVME8100 power distribution structure.

*Figure 4-5 Power Distribution*



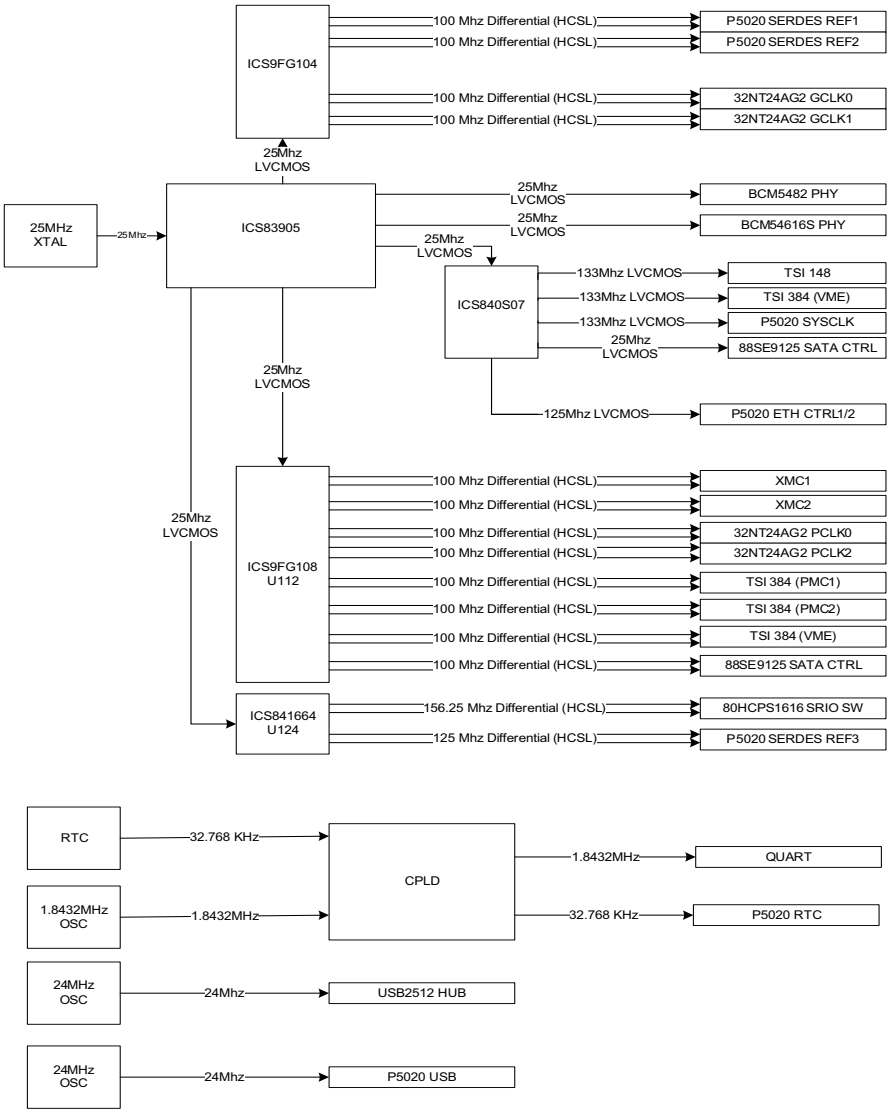

## 4.20.2 Power Sequence Requirements

The CPLD power sequence timing is designed to support all the MVME8100 devices supply voltage sequencing requirements.

# 4.21 Clock Structure

Figure 4-7 shows the clock tree implementation for the MVME8100.

*Figure 4-6 Clock Structure*

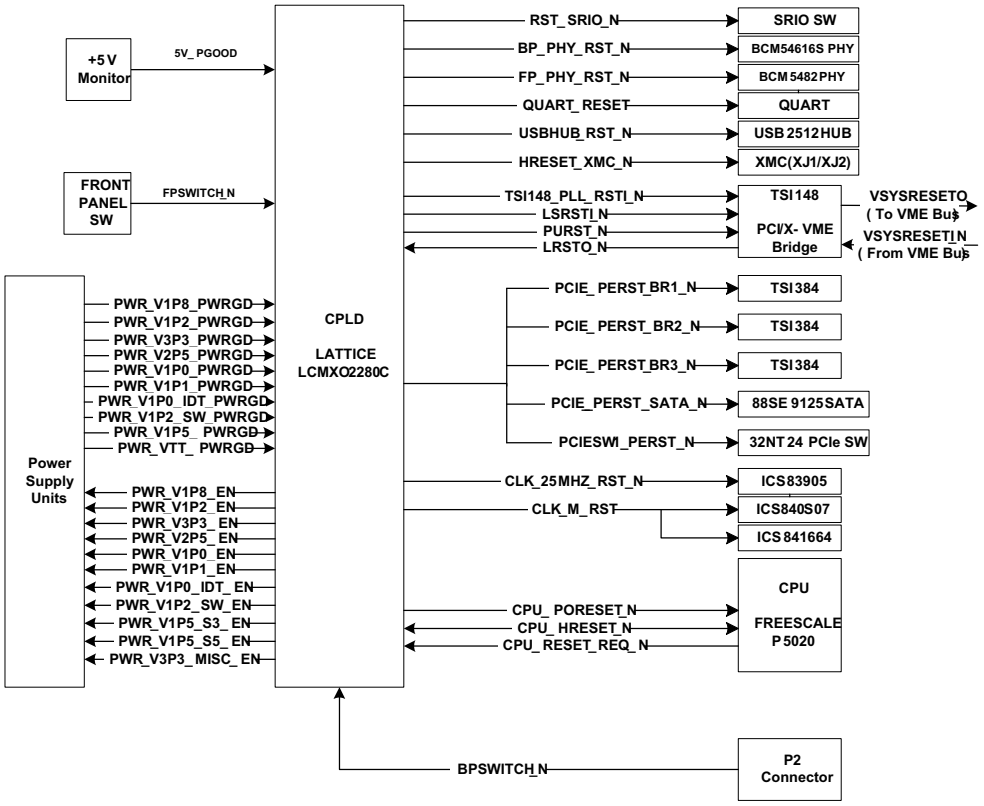


## 4.22 Reset Structure

The MVME8100 reset begins after the power up sequence is completed. A board reset can also be initiated using the front panel reset switch, the RTM reset switch (through P2) or under software control through the processor Reset Request.

Figure 4-7 illustrates the reset control structure.

*Figure 4-7 Reset Control Diagram*



# 4.23 Interrupt Controller Assignments

The following table shows the external interrupts connected to the P5020:

*Table 4-1 P5020 External Interrupt Assignments*

| P5020 Interrupt | Interrupt Source | Description |
|---|---|---|
| IRQ0 | None | Reserved |
| IRQ1 | BCM5482 INT1 | BCM5482 PHY interrupt 1 from LED_P1[2] pin |
| IRQ2 | BCM5482 INT2 | BCM5482 PHY interrupt 2 from LED_P2[2] pin |
| IRQ3/GPIO21 | QUART_IRQ0 | Quart Interrupt INTA |
| IRQ4/GPIO22 | QUART_IRQ1 | Quart Interrupt INTB |
| IRQ5/GPIO23 | QUART_IRQ2 | Quart Interrupt INTC |
| IRQ6/GPIO24 | QUART_IRQ3 | Quart Interrupt INTD |
| IRQ7/GPIO25 | CPLD_TEMP_INT_L | Board Temperature interrupt (routed through CPLD) |
| IRQ8/GPIO26 | CPLD_TIMER_INT_L | CPLD Internal Timers and Abort IRQ |
| IRQ9/GPIO27 | BCM54616S INT | BCM54616S PHY interrupt from LED4 pin. |
| IRQ10/GPIO28 | SRIO_IRQ_INT_L | 80HCPS1616 SRIO IRQ_N pin |
| IRQ11/GPIO29 | RTC_INT_L | RTC interrupt (routed through CPLD) |

## 4.24 GPIO Electrical Characteristics

The four GPIO signals routed to the P0 and P2 connectors have the following electrical characteristics:

*Table 4-2 GPIO DC Electrical Characteristics*

| $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max.(V) | $V_{OH}$ Min.(V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|
| Min.(V) | Max.(V) | Min.(V) | Max.(V) | | | | |
| -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | 2.9 | 4 | 4 |
| | | | | 0.2 | 3.1 | 0.1 | 0.1 |

*Table 4-3 GPIO Pull-Down Characteristics*

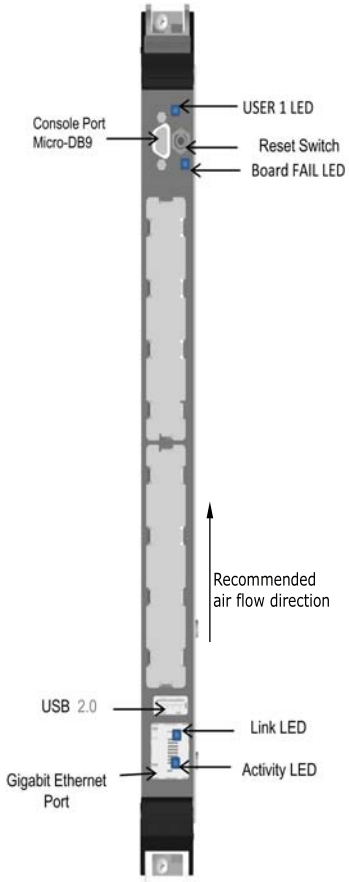
| Parameter | Condition | Min. | Max | Units |
|---|---|---|---|---|
| I/O Active Pull-down Current | $V_{IL}$ (Max) ≤ $V_{IN}$ ≤ $V_{IH}$ (Max) | 30 | 150 | uA |

## 4.25 Thermal Management

The MVME8100 provides three on-board temperature sensors using an ADT7461 dual temperature sensor and a TMP112A temperature sensor. The ADT7461 internal temperature sensor provides the temperature at the board edge on the CPU side of the board. The ADT7461 remote temperature sensor measures the CPU temperature. The ADT7461 can measure negative temperatures down to -64C with +/- 1C accuracy on the remote sensor and +/- 3C accuracy on the internal sensor. The ADT7461 registers can be used to configure the low temperature limit and high temperature limit for the local sensor as well as for the remote sensor. An interrupt can be generated if limits are exceeded. The TMP112A temperature sensor is used to measure the temperature at the board edge opposite from the CPU. Since the airflow direction can be different in some VME chassis, either temperature sensor can be used to get a measure of the board inlet air temperature, depending on the air flow direction.

However, to maintain proper CPU temperature, the recommended air flow direction is to enter the board from the CPU side, that is, the air should flow in the direction from PMC/XMC site 1 to PMC/XMC Site 2.

*Figure 4-8 Thermal Management*



# Boot System

## 5.1 Overview

The MVME8100 uses Das U-Boot, a boot loader software based on the GNU Public License. It boots the blade and is the first software to be executed after the system is powered on.

Its main functions are:

- Initialize the hardware
- Pass boot parameters to the Linux kernel
- Start the Linux kernel
- Update Linux kernel and U-Boot images

This section describes U-Boot features and procedures that are specific to the MVME8100 . For general information on U-Boot, see http://www.denx.de/wiki/UBoot/WebHome.

## 5.2 Accessing U-Boot

1. Connect the board to a computer with a serial interface connector and a terminal emulation software running on it. The serial connector of the board is found on the face plate.
2. Configure the terminal software to use the access parameters that are specified in U-Boot. By default, the access parameters are as follows:
   - Baud rate: 9600
   - PC ANSI
   - 8 data bits
   - No parity
   - 1 stop bit

These serial access parameters are the default values. These can be changed from within the U-Boot. For details, refer to the U-Boot documentation.

3. Boot the MVME8100 .
4. When prompted, press the "Ctrl/C" key.

U-Boot aborts the boot sequence and enters into a command line interface mode.

Enter the command **`setenv bootdelay -1; saveenv`** to disable the U-Boot auto-boot feature and let the U-Boot directly enter the command line interface after the next reboot/power up.

## 5.3 Boot Options

### 5.3.1 Booting from a Network

In this mode, U-Boot downloads and boots the Linux kernel from an external TFTP server and mounts a root file system located on a network server.

1. Make sure that the `kernel, dtb,` and `ramdisk` are accessible to the board from the TFTP server.

2. Configure U-Boot environment variables:

```
setenv ipaddr <IP address of MVME8100>
setenv serverip <IP address of TFTP server>
setenv gatewayip <gateway IP>
setenv netmask <netmask>
setenv bootargs 'root=/dev/ram rw console=ttyS0,9600n8
ramdisk_size=700000 cache-sram-size=0x10000'
saveenv
```

3. Transfer the files through the TFTP from the server to the local memory.

```
tftp 1000000 <kernel_image>
tftp 2000000 <ramdisk>
tftp f00000 <kernel dtb>
```

4. Boot the Linux from the memory.

```
bootm 1000000 2000000 f00000
```

### 5.3.2 Booting from an Optional SATA Drive

1. Make sure that the `kernel, dtb,` and `ramdisk` are saved in the SATA drive with ext2 partition.
2. Configure U-Boot environment variable:
```
setenv File_uImage <kernel_image>
setenv File_dtp <kernel dtb>
setenv File_ramdisk <ramdisk>
saveenv
```
3. Copy the files from the SATA drive to the memory:
```
# option: scsi - interface, 0:1 - device 0 partition 1
ext2load scsi 0:1 1000000 $File_uImage
ext2load scsi 0:1 2000000 $File_ramdisk
ext2load scsi 0:1 f00000 $File_dtp
```
4. Boot the Linux in memory.
```
bootm 1000000 2000000 f00000
```

### 5.3.3 Booting from a USB Drive

1. Make sure that the `kernel, dtb`, and `ramdisk` are saved in the USB drive with FAT partition.
2. Configure the U-Boot environment variable:
```
setenv File_uImage <kernel_image>
setenv File_dtp <kernel dtb>
setenv File_ramdisk <ramdisk>
saveenv
```
3. Initialize USB drive:
```
usb start
```
4. Load the files from the USB drive to the memory:
```
# option: usb - interface, 0:1 - device 0 partition 1
fatload usb 0:1 1000000 $File_uImage
fatload usb 0:1 2000000 $File_ramdisk
fatload usb 0:1 f00000 $File_dtb
```
5. Boot the Linux in memory:
```
bootm 1000000 2000000 f00000
```

### 5.3.4 Booting from eMMC

1. Make sure that the `kernel, dtb`, and `ramdisk` are saved in the onboard eMMC device with FAT partition.
2. Configure the U-Boot environment variable:
```
setenv File_uImage <kernel_image>
setenv File_dtp <kernel dtb>
setenv File_ramdisk <ramdisk>
saveenv
```
3. Initialize eMMC
```
mmcinfo
```
4. Load the files from the eMMC to the memory:
```
# option: mmc - interface, 0:1 - device 0 partition 1
fatload mmc 0:1 1000000 $File_uImage
fatload mmc 0:1 2000000 $File_ramdisk
fatload mmc 0:1 f00000 $File_dtp
```
5. Boot the Linux in memory:
```
bootm 1000000 2000000 f00000
```

### 5.3.5 Booting VxWorks Through the Network

In this mode, the U-Boot downloads and boots VxWorks from an external TFTP server.

1. Make sure that the VxWorks image is accessible by the board from the TFTP server.
2. Configure U-Boot environment variables:
```
setenv ipaddr <IP address of MVME8100>
setenv serverip <IP address of TFTP server>
setenv gatewayip <gateway IP>
setenv netmask <netmask>
setenv vxboot 'tftpboot $vxbootfile && setenv bootargs
$vxbootargs && bootvx'
setenv vxbootfile <VxWorks_image>
setenv vxbootargs 'dtsec(3,0)<IP address of TFTP server>:VxWorks
h=<IP address of TFTP server> e=<IP address of MVME8100>:ffffff00
b=<unused IP> u=vxworks pw=vxworks f=0x80'
saveenv
```

3. TFTP the files from the server to local memory, then boot:
   ```
   run vxboot
   ```

## 5.4 MVME8100 Specific U-Boot Commands

*Table 5-1 MVME8100 Specific U-Boot Commands*

| Command | Description |
|---|---|
| base | Print or set address offset |
| bdinfo | Print board info structure |
| boot | Boot default, i.e., run 'bootcmd' |
| bootd | Boot default, i.e., run 'bootcmd' |
| bootelf | Boot from an ELF image in memory |
| bootm | Boot application image from memory |
| bootp | Boot image through network using BOOTP/TFTP protocol |
| bootvx | Boot VxWorks from an ELF image |
| cmp | Memory compare |
| coninfo | Print console devices and information |
| cp | Memory copy |
| cpu | Multiprocessor CPU boot manipulation and release |
| crc32 | Checksum calculation |
| date | Get/set/reset date & time |
| diags | Runs POST diags |
| echo | Echo args to console |
| exit | Exit script |
| ext2load | Load binary file from a Ext2 file system |
| ext2ls | List files in a directory (default /) |
| fatinfo | Print information about file system |
| fatload | Load binary file from a DOS file system |

*Table 5-1 MVME8100 Specific U-Boot Commands (continued)*

| Command | Description |
|---|---|
| fatls | List files in a directory (default /) |
| fdt | Flattened device tree utility commands |
| go | Start application at address 'addr' |
| help | Print online help |
| i2c | I2C sub-system |
| iminfo | Print header information for application image |
| imxtract | Extract a part of a multi-image |
| interrupts | Enable or disable interrupts |
| itest | Return true/false on integer compare |
| loadb | Load binary file over serial line (kermit mode) |
| loads | Load S-Record file over serial line |
| loady | Load binary file over serial line (ymodem mode) |
| loop | Infinite loop on address range |
| md | Memory display |
| memmap | Displays memory map |
| mii | MII utility commands |
| mm | Memory modify (auto-incrementing address) |
| mmc | MMC sub system |
| mmcinfo | Display MMC info |
| moninit | Reset nvram, serial#, and write monitor to SPI flash |
| mtest | Simple RAM read/write test |
| mw | Memory write (fill) |
| nfs | Boot image through network using NFS protocol |
| nm | Memory modify (constant address) |
| pci | List and access PCI Configuration Space |
| pci_info | Show information about devices on PCI bus |
| ping | Send ICMP ECHO_REQUEST to network host |

*Table 5-1 MVME8100 Specific U-Boot Commands (continued)*

| Command | Description |
|---|---|
| printenv | Print environment variables |
| rarpboot | Boot image through network using RARP/TFTP protocol |
| reset | Perform RESET of the CPU |
| run | Run commands in an environment variable |
| saveenv | Save environment variables to persistent storage |
| script | Run a ';' delimited, ';;' terminated list of commands |
| scsi | SCSI sub-system |
| scsiboot | Boot from SCSI device |
| setenv | Set environment variables |
| setexpr | Set environment variable as the result of eval expression |
| sf | SPI flash sub-system |
| showvar | Print local hushshell variables |
| sleep | Delay execution for some time |
| soft_reset | Soft reset the board |
| source | Run script from memory |
| test | Minimal test like /bin/sh |
| tftpboot | Boot image through network using TFTP protocol |
| tsi148 | Initialize and configure Tundra Tsi148 |
| usb | USB sub-system |
| usbboot | Boot from USB device |
| version | Print monitor version |

## 5.5 Updating U-Boot

To update the U-Boot, place the image in the RAM (address 0x1000000 in this example) before copying it to the SPI flash.

The following procedure will replace the image in SPI bank 0:

1. Ensure FLASH_WP_N in SMT Configuration Switch (S3-1) is in the "OFF" position.
2. Select SPI flash # 0:
   ```
   sf probe 0
   ```
3. Erase 0x90000 bytes starting at SPI address 0:
   ```
   sf erase 0 0x90000
   ```
4. Write 0x90000 bytes from RAM address 0x1000000 starting at SPI address 0:
   ```
   sf write 0x1000000 0 0x90000
   ```

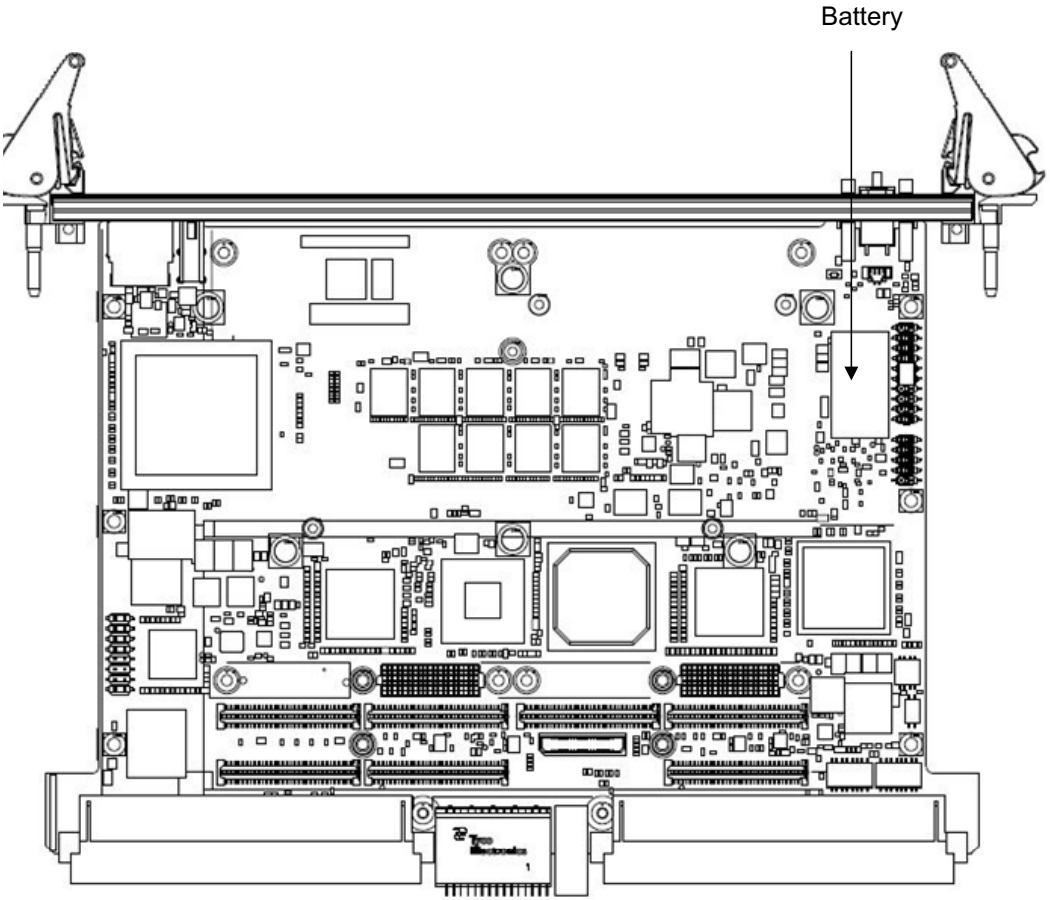
To replace the image in SPI bank 1, replace step 2 with Select SPI flash # 1:

```
sf probe 1
```

## A.1 Battery Exchange

The ENP1 variant contains an on-board battery. The battery location is shown in the following figure.

*Figure A-1 Battery Location*



The battery provides data retention of seven years summing up all periods of actual data use. Emerson therefore assumes that there usually is no need to exchange the battery except, for example, in case of long-term spare part handling.

**NOTICE**

Board/System Damage
Incorrect exchange of lithium batteries can result in a hazardous explosion.
When exchanging the on-board lithium battery, make sure that the new and the old battery are exactly the same battery models.
If the respective battery model is not available, contact your local Emerson sales representative for the availability of alternative, officially approved battery models.

Data Loss
Exchanging the battery can result in loss of time settings. Backup power prevents the loss of data during exchange.
Quickly replacing the battery may save time settings.

Data Loss
If the battery has low or insufficient power the RTC is initialized.
Exchange the battery before seven years of actual battery use have elapsed.

PCB and Battery Holder Damage
Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent damage, do not use a screw driver to remove the battery from its holder.

### Exchange Procedure

To exchange the battery, proceed as follows:

1. Remove the old battery.
2. Install the new battery with the plus sign (+) facing up.
3. Dispose of the old battery according to your country's legislation and in an environmentally safe way.

# Related Documentation

## B.1 Emerson Network Power - Embedded Computing Documents

The publications listed below are referenced in this manual. You can obtain electronic copies of Emerson Network Power - Embedded Computing publications by contacting your local Emerson sales office. For released products, you can also visit our Web site for the latest copies of our product documentation.

1. Go to www.Emerson.com/EmbeddedComputing.The Emerson Embedded Computing website opens.
2. Click on Technical Documentation link.
3. Click on Search Our Technical Documentation Archive link.
4. In the Search box, type the publication number of the manual you are looking for.

*Table B-1 Emerson Network Power - Embedded Computing Publications*

| Document Title | Publication Number |
|---|---|
| MVME8100 Programmer's Reference | 6806800P28 |
| MVME8100 Quick start Guide | 6806800P26 |
| MVME8100 Safety Notes Summary | 6806800P27 |

## B.2 Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

*Table B-2 Related Specifications*

| Organization and Standard | Document Title |
|---|---|
| VITA Standards Organization | |
| VME64 | ANSI/VITA 1-1994 |
| VME64 Extensions | ANSI/VITA 1.1-1997 |

*Table B-2 Related Specifications (continued)*

| Organization and Standard | Document Title |
|---|---|
| 2eSST Source Synchronous Transfer | ANSI/VITA 1.5-2003 |
| Processor PMC | ANSI/VITA 32-2003 |
| PCI-X for PMC and Processor PMC | ANSI/VITA 39-2003 |
| XMC Switched Mezzanine Card Auxiliary Standard, September 2005 | VITA 42.0-2005 |
| XMC PCI Express Protocol Layer Standard, June 2006 | VITA 42.3-2006 |
| Conduction Cooled PMC | ANSI/VITA 20 - 2001 |
| PMC I/O Module (PIM) Draft Standard | VITA 36<br>Draft Rev 0.1<br>July 19, 1999 |
| Universal Serial Bus | |
| Universal Serial Bus Specification | Revision 2.0<br>April 27, 2000 |
| PCI Special Interest Group | |
| PCI Local Bus Specification, Revision 2.2 | PCI Rev 2.2<br>December 18, 1998 |
| PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification, Revision 2.0a | PCI-X EM 2.0a<br>August 22, 2003 |
| PCI-X Protocol Addendum to the PCI Local Bus Specification, Revision 2.0a | PCI-X PT 2.0a<br>July 22, 2003 |
| Institute for Electrical and Electronics Engineers, Inc. | |
| IEEE Standard for a Common Mezzanine Card Family: CMC | IEEE1386<br>Oct 25, 2001 |
| IEEE Standard Physical and Environmental Layer for PCI Mezzanine Cards: PMC | IEEE1386.1<br>Oct 25, 2001 |
| Conduction cooled VME mechanics | IEEE 1101.2 - 1992 |
| Additional Mechanical Specifications | IEEE 1101.10 - 1996 |
| IEEE Standard for Mechanical Core Specifications for Microcomputers | IEEE 1101.1 - 1998 |

# B.3 Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

*Table B-3 Manufacturer's Publications*

| Document Title and Source | Publication Number |
|---|---|
| Freescale Corporation | |
| P5020/P5010 QorIQ Integrated Processor Hardware Specifications | P5020EC |
| P5020 QorIQ Integrated Multicore Communication Processor Reference Manual | P5020RM |
| Integrated Devices | |
| IDT 89HPES32NT24xG2 PCI Express Switch User Manual | |
| CPS-1616 User Manual | |

# Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

Emerson intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your Emerson representative.

This product is a Safety Extra Low Voltage (SELV) device designed to meet the EN60950-1 requirements for Information Technology Equipment. The use of the product in any other application may require safety evaluation specific to that application.

Only personnel trained by Emerson or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product.

The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local Emerson representative for service and repair to make sure that all safety features are maintained.

## EMC

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications.

Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense. Changes or modifications not expressly approved by Emerson Network Power could void the user's authority to operate the equipment. Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a compliant system will maintain the required performance. Use only shielded cables when connecting peripherals to assure that appropriate radio frequency emissions compliance is maintained.

## Operation

Product Damage
High humidity and condensation on the board surface causes short circuits.
Do not operate the board outside the specified environmental limits.
Make sure the board is completely dry and there is no moisture on any surface before applying power.

Damage of Circuits
Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.
Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

Board Malfunction
Switches marked as “reserved” might carry production-related functions and can cause the board to malfunction if their setting is changed.
Do not change settings of switches marked as “reserved”. The setting of switches which are not marked as “reserved” has to be checked and changed before board installation.

## Installation

Data Loss
Powering down or removing a board before the operating system or other software running on the board has been properly shut down may cause corruption of data or file systems. Make sure all software is completely shut down before removing power from the board or removing the board from the chassis.

Product Damage
Only use injector handles for board insertion to avoid damage to the front panel and/or PCB. Deformation of the front panel can cause an electrical short or other board malfunction.

Product Damage
Inserting or removing modules with power applied may result in damage to module components.
Before installing or removing additional devices or modules, read the documentation that came with the product.

## Cabling and Connectors

Product Damage
RJ-45 connectors on modules are either twisted-pair Ethernet (TPE) or E1/T1/J1 network interfaces. Connecting an E1/T1/J1 line to an Ethernet connector may damage your system.

- Make sure that TPE connectors near your working area are clearly marked as network connectors.
- Verify that the length of an electric cable connected to a TPE bushing does not exceed 100 meters.
- Make sure the TPE bushing of the system is connected only to safety extra low voltage circuits (SELV circuits).

If in doubt, ask your system administrator.

## Battery

Board/System Damage

Incorrect exchange of lithium batteries can result in a hazardous explosion.

When exchanging the on-board lithium battery, make sure that the new and the old battery are exactly the same battery models.

If the respective battery model is not available, contact your local Emerson sales representative for the availability of alternative, officially approved battery models.

Data Loss
Exchanging the battery can result in loss of time settings. Backup power prevents the loss of data during exchange.
Quickly replacing the battery may save time settings.

Data Loss
If the battery has low or insufficient power the RTC is initialized.
Exchange the battery before seven years of actual battery use have elapsed.

PCB and Battery Holder Damage
Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent damage, do not use a screw driver to remove the battery from its holder.

# Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Produktes innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am Produkt zur Folge haben.

Emerson ist darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem Produkt in diesem Handbuch bereit zu stellen. Da es sich jedoch um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von Emerson.

Das Produkt wurde entwickelt, um die Sicherheitsanforderungen für SELV Geräte nach der Norm EN 60950-1 für informationstechnische Einrichtungen zu erfüllen. Die Verwendung des Produkts in einer anderen Anwendung erfordert eine Sicherheitsüberprüfung für diese spezifische Anwendung.

Einbau, Wartung und Betrieb dürfen nur von durch Emerson ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

Halten Sie sich von stromführenden Leitungen innerhalb des Produktes fern. Entfernen Sie auf keinen Fall Abdeckungen am Produkt. Nur werksseitig zugelassenes Wartungspersonal oder anderweitig qualifiziertes Wartungspersonal darf Abdeckungen entfernen, um Komponenten zu ersetzen oder andere Anpassungen vorzunehmen.

Installieren Sie keine Ersatzteile oder führen Sie keine unerlaubten Veränderungen am Produkt durch, sonst verfällt die Garantie. Wenden Sie sich für Wartung oder Reparatur bitte an die für Sie zuständige Geschäftsstelle von Emerson. So stellen Sie sicher, dass alle sicherheitsrelevanten Aspekte beachtet werden.

## EMV

Das Produkt wurde in einem Emerson Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Produktes in Gewerbe- sowie Industriegebieten gewährleisten.

Das Produkt arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.

Wird das Produkt in einem Wohngebiet betrieben, so kann dies mit grosser Wahrscheinlichkeit zu starken Störungen führen, welche dann auf Kosten des Produktanwenders beseitigt werden müssen. Änderungen oder Modifikationen am Produkt, welche ohne ausdrückliche Genehmigung von Emerson Network Power durchgeführt werden, können dazu führen, dass der Anwender die Genehmigung zum Betrieb des Produktes verliert.  Boardprodukte werden in einem repräsentativen System getestet, um zu zeigen, dass das Board den oben aufgeführten EMV-Richtlinien entspricht. Eine ordnungsgemässe Installation in einem System, welches die EMV-Richtlinien erfüllt, stellt sicher, dass das Produkt gemäss den EMV-Richtlinien betrieben wird. Verwenden Sie nur abgeschirmte Kabel zum Anschluss von Zusatzmodulen. So ist sichergestellt, dass sich die Aussendung von Hochfrequenzstrahlung im Rahmen der erlaubten Grenzwerte bewegt.

Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.

## Betrieb

1  Beschädigung des Produktes
Hohe Luftfeuchtigkeit und Kondensat auf der Oberfläche des Produktes können zu Kurzschlüssen führen.
Betreiben Sie das Produkt nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Produkt kein Kondensat befindet.

Beschädigung von Schaltkreisen
Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau des Produktes kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.
Bevor Sie das Produkt oder elektronische Komponenten berühren, vergewissern Sie sich, daß Sie in einem ESD-geschützten Bereich arbeiten.

Fehlfunktion des Produktes
Schalter, die mit 'Reserved' gekennzeichnet sind, können mit produktionsrelevanten Funktionen belegt sein. Das Ändern dieser Schalter kann im normalen Betrieb Störungen auslösen.
Verstellen Sie nur solche Schalter, die nicht mit 'Reserved' gekennzeichnet sind. Prüfen und ggf. ändern Sie die Einstellungen der nicht mit 'Reserved' gekennzeichneten Schalter, bevor Sie das Produkt installieren.

## Installation

Datenverlust
Das Herunterfahren oder die Deinstallation eines Boards bevor das Betriebssystem oder andere auf dem Board laufende Software ordnungsmemäss beendet wurde, kann zu partiellem Datenverlust sowie zu Schäden am Filesystem führen.
Stellen Sie sicher, dass sämtliche Software auf dem Board ordnungsgemäss beendet wurde, bevor Sie das Board herunterfahren oder das Board aus dem Chassis entfernen.

Beschädigung des Produktes
Fehlerhafte Installation des Produktes kann zu einer Beschädigung des Produktes führen.
Verwenden Sie die Handles, um das Produkt zu installieren/deinstallieren. Auf diese Weise vermeiden Sie, dass das Face Plate oder die Platine deformiert oder zerstört wird.

Beschädigung des Produktes und von Zusatzmodulen
Fehlerhafte Installation von Zusatzmodulen, kann zur Beschädigung des Produktes und der Zusatzmodule führen.
Lesen Sie daher vor der Installation von Zusatzmodulen die zugehörige Dokumentation.

## Kabel und Stecker

Beschädigung des Produktes
Bei den RJ-45-Steckern, die sich an dem Produkt befinden, handelt es sich entweder um Twisted-Pair-Ethernet (TPE) oder um E1/T1/J1-Stecker. Beachten Sie, dass ein versehentliches Anschließen einer E1/T1/J1-Leitung an einen TPE-Stecker das Produkt zerstören kann.

- Kennzeichnen Sie deshalb TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes deutlich als Netzwerkanschlüsse.
- Stellen Sie sicher, dass die Länge eines mit Ihrem Produkt verbundenen TPE-Kabels 100 m nicht überschreitet.
- Das Produkt darf über die TPE-Stecker nur mit einem Sicherheits-Kleinspannungs-Stromkreis (SELV) verbunden werden.

Bei Fragen wenden Sie sich an Ihren Systemverwalter.

## Batterie

Beschädigung des Blades

Ein unsachgemäßer Einbau der Batterie kann gefährliche Explosionen und

Beschädigungen des Blades zur Folge haben.

Verwenden Sie deshalb nur den Batterietyp, der auch bereits eingesetzt wurde und

befolgen Sie die Installationsanleitung.

Datenverlust
Wenn Sie die Batterie austauschen, können die Zeiteinstellungen verloren gehen. Eine Backupversorgung verhindert den Datenverlust während des Austauschs.
Wenn Sie die Batterie schnell austauschen, bleiben die Zeiteinstellungen möglicherweise erhalten.

Datenverlust
Wenn die Batterie wenig oder unzureichend mit Spannung versorgt wird, wird der RTC initialisiert.
Tauschen Sie die Batterie aus, bevor sieben Jahre tatsächlicher Nutzung vergangen sind.

Schäden an der Platine oder dem Batteriehalter
Wenn Sie die Batterie mit einem Schraubendreher entfernen, können die Platine oder der Batteriehalter beschädigt werden.
Um Schäden zu vermeiden, sollten Sie keinen Schraubendreher zum Ausbau der Batterie verwenden.

## Umweltschutz

Entsorgen Sie alte Batterien und/oder Blades/Systemkomponenten/RTMs stets gemäß der in Ihrem Land gültigen Gesetzgebung, wenn möglich immer umweltfreundlich.

## HOW TO REACH LITERATURE AND TECHNICAL SUPPORT:

For literature, training, and technical assistance and support programs, visit
www.emersonnetworkpower.com/embeddedcomputing

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- Connectivity
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- Outside Plant
- Power Switching & Control
- Precision Cooling
- Services
- Site Monitoring
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